Yield Comparison of Die-first Face-Down and Die-last Fan-out Wafer Level Packaging

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***Abstract*—This analysis focuses on two of the primary variations of fan-out wafer level packaging: die-first packaging in which the die are placed face down, and die-last packaging. These two technologies share many of the same activities, but those activities occur in a different order. One key factor setting these two process flows apart is yield. Even with the assumption that the same level of defects are introduced in each process flow, the resulting total yield differs.**

This paper analyzes the impact of defects on the die-first and die-last processes. Each process is evaluated separately, then the two processes are directly compared across a range of designs, defect density assumptions, and incoming die cost assumptions. The cost of the processing, cost of the incoming die, and the cost of processing and die lost to scrap are included.

Keywords—die-first face-down, die-last, fan-out wafer level packaging, yield

I. INTRODUCTION

There are many process flows on the market or coming to market that are captured under the fan-out wafer level packaging (WLP) umbrella [1]. The first major technology in the fan-out WLP family was embedded wafer level ball grid array (eWLB), introduced by Infineon in the mid-2000's [2]. eWLB is an example of a fan-out WLP process in which the die is placed before redistribution layer (RDL) creation, and that die is placed face-down. Another variation on die-first processing exists, in which the die is placed face-up instead of face-down. That variation is not included in this comparison, but shares many of the same characteristics as the face-down version analyzed.

Since the introduction of eWLB and other die-first fan-out technologies, processes in which the die is placed after RDL creation have also been introduced. These processes can seem reminiscent of flip chip technology, since the interconnect is built up first, and then the die is placed. Even so, they are typically called die-last (or RDL-first) styles of fan-out.

This analysis focuses on die-first face down and die-last processing. The process flows for both of these technologies are shown in Fig. 1 and 2 on the next page.

As seen in the process flows, die-first and die-last processing share many of the same activities, but those activities occur in a different order. The shared activities include mold application, redistribution layer (RDL) creation, solder ball attach, and die placement activities.

However, there are a few activities that are unique to each process flow. For example, in die-last processing, RDL formation is one of the first activities to occur, which means a surface must be provided upon which to form that RDL. This is in contrast to die-first processing, where mold is used to create a reconstituted wafer, and the RDL is patterned and imaged on that reconstituted wafer. The die-last process requires a special carrier at the beginning of the process. Later in the process, that carrier must then be removed when the fan-out package is nearing completion. While die-first processing does involve carrier-like steps, in that the die are placed on a carrier of double-sided tape before the mold is applied to create the reconstituted wafer, the activities are simple. The carrier and debond steps associated with die-last processing are more complex [3].

Another difference between the two variations is that the die coming into the die-last process must come in with bumps or copper pillars, which requires additional processing of the incoming wafer.

The mold process may also differ between die-first and die-last processing. In die-first processing, the wafer is compression molded. In die-last processing, capillary underfill may be applied after die placement and then the wafer may be compression molded, or a molded underfill approach may be used [4,5].

These are not all of the differences between these two categories of fan-out WLP, but they are an indication that any direct comparison has components beyond yield that must be quantified.

II. PACKAGING COST

A. Processing Cost Differences

Although the focus of this analysis is the impact of yield, the packaging cost must also be taken into consideration. As stated above, die-first and die-last processing share many of the same activities, but not all. Overall, the processing cost of die-last tends to be more expensive than die-first. One major reason is the fact that die being placed in a die-last package must have bumps, copper pillars, or copper studs. This means that a wafer coming in for fan-out packaging will

have additional processing required before it can be used in a die-last package. On the other hand, that same wafer can simply be diced and placed in a die-first package. This additional wafer processing shows up as an added material cost in the die-last process.

Additionally, the carrier wafer and subsequent debond process required for die-last processing are more expensive than the simple lamination and delamination that occur early in the die-first process.

There are other areas in which the processing costs of activities may differ between the flows. Different throughput or material assumptions, or the inclusion of extra inspection steps, will account for small differences. However, the requirement for bumping and for a robust support wafer and debond process tend to mean that die-last processing costs are higher than for an equivalent die-first package. That fact will be taken into account in the direct yield comparisons.

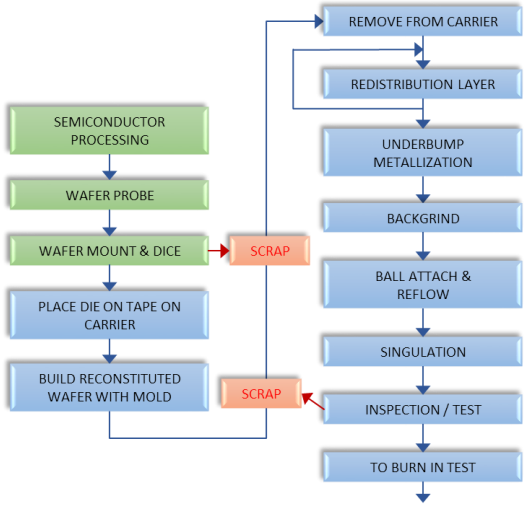

Figure 1. Die-first face-down process flow

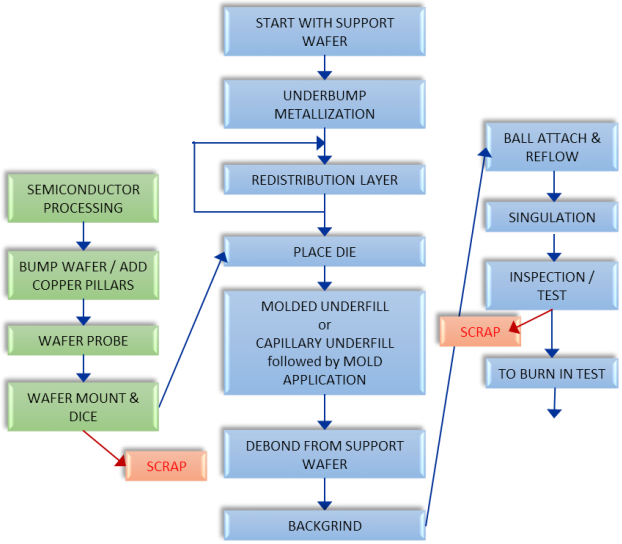

Figure 2. Die-last process flow

B. *Activity Based Cost Modeling*

Activity based cost modeling was used to construct generic die-first face-down and die-last fan-out WLP cost models. With activity based cost modeling, a process flow is divided into a series of activities, and the total cost of each activity is calculated. The following cost components are analyzed for each activity.

- Equipment cost and throughput – The throughput determines how long a wafer consumes the equipment. The total equipment cost determines how much depreciation should be allocated based on how long the equipment is consumed.
- Labor cost – The activity time and percentage of an operator required determine the labor component of the activity.
- Material cost – Both permanent material costs and consumable material costs are included. Permanent material includes mold, dielectric layers, copper, solder balls, etc. Consumables include chemicals for cleaning, flux, etch baths, etc.
- Yield loss – The cost of scrapped packages is allocated to the remaining good packages.
- Overhead and indirect costs – Typical overhead and indirect costs are accounted for.

Note that no overhead or indirect assumptions are made for either the die-first or die-last cost models used in this analysis.

Fig. 3 gives an example of the level of detailed output provided by an activity based cost model. The chart shows the first few steps of a die-first fan-out wafer level packaging process. The type of cost associated with each activity is broken down by color. In the steps selected, it can be seen that there is a high capital cost associated with the die bond step, and a high material cost associated with the compression molding step. The category labelled "macro" in the chart refers to the overhead and indirect cost assumptions. It can be seen that these are amortized over the entire process, allocated to each step.

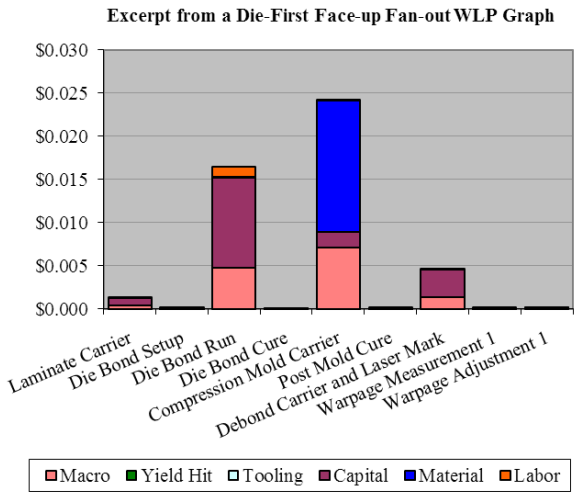

Figure 3. Example of activity based cost modeling output

III. Yield Considerations

There are a variety of activities that may introduce defects during fan-out wafer level processing.

In die-first processing, one key area that may affect yield is die shift due to mold. The application of the mold may shift the die from where it is expected to be [6]. Curing the mold may also shift the die. Wafer warpage is also a concern—if the reconstituted wafer upon which the RDL will be formed is warped, RDL processing will be more difficult and more prone to defects.

In die-last processing, debonding the nearly-finished product from a support wafer is a risk area where defects may be introduced. Mechanical stress, temperatures that are too high, or improperly removed adhesive material are all examples of opportunities for yield impact during debonding.

In both process flows, RDL creation and ball attach are two key points when defects may be introduced. The multitude of material and imaging steps used for RDL creation are the main reason there is the potential for a yield impact. Ball attach has the potential to introduce defects because of the precision required when placing the solder balls.

The timing of defect introduction is a key point when comparing die-first and die-last processing. When a defect is introduced after the die has been placed, it is not only the cost of processing up until that point that will be lost, but the die will be lost as well. A die is placed much earlier in the die-first process, which means the die-first process is susceptible to a higher yield hit. This is in contrast to the die-last process, in which the die is placed after RDL creation. Any defects introduced during the RDL creation process will not result in the loss of die if the die are placed only on known good RDL locations.

Although the die-first and die-last process flows have different steps, which means a different level of defects may be introduced, for the purposes of this analysis, the same number of defects are assumed to be introduced in both processes. This allows for an apples to apples yield comparison. The three activities that introduce defects in both of these cost models are RDL creation, die placement, and ball attach.

One variation in the process flows not yet addressed, which may have an impact on yield, is the type of RDL creation process selected. There are multiple ways that an RDL can be formed, and each type of RDL creation will bring different yield assumptions (along with different line and space capabilities and other considerations). Options for RDL creation involve a dual damascene process, an RDL built on a typical wafer bumping line, or a laser direct imaging process. The cost models used in this analysis assume not only the same defect assumptions for all steps that introduce defects, but the same style of RDL creation as well. This means the cost of RDL creation in both varieties of fan-out compared is approximately equivalent.

IV. Single Process Yield Analysis

The impact of defects on die-first and die-last processes were analyzed separately before a direct comparison was carried out.

A. *Die-first Face-down*

Table I outlines small, medium, and large designs that will be utilized throughout the analysis. These are all single-RDL designs. Table II shows the impact of defects introduced in a die-first fan-out process for these designs.

TABLE I. Designs

Package Size	***Die size***	***I/O Count***	***# of RDLs***
5mmx5mm	3mmx3mm	160	1
8mmx8mm	5mmx5mm	460	1
12mmx12mm	9mmx9mm	1060	1

The impact on cost is shown as a percent increase. In addition to showing the defect density assumptions, the total process yield that results from those defect density assumptions is included. The cost calculations take into account the cost of the packaging process, the cost of the die being packaged, and the cost of scrapping a bad package (including scrapping the die in that package).

TABLE II. Die-first Results

Additional Defects per cm^2	***5mmx5mm package, 3mmx3mm die***	
	Resulting Total Yield	***% Cost Increase from Baseline***
0.00	99.43%	0.00%
0.02	98.94%	0.48%
0.04	98.45%	0.97%
0.06	97.97%	1.46%
0.08	97.48%	1.91%
Additional Defects per cm^2	***8mmx8mm package, 5mmx5mm die***	
	Resulting Total Yield	***% Cost Increase from Baseline***
0.00	98.54%	0.00%
0.02	97.30%	1.23%
0.04	96.06%	2.45%
0.06	94.85%	3.65%
0.08	93.64%	4.87%
Additional Defects per cm^2	***12mmx12mm package, 9mmx9mm die***	
	Resulting Total Yield	***% Cost Increase from Baseline***
0.00	96.75%	0.00%
0.02	94.01%	2.67%
0.04	91.34%	5.26%
0.06	88.75%	7.79%
0.08	86.24%	10.25%

The first row in Table II, which has zero additional defects and zero percent, is the baseline. Note that the 0.0 defect density assumption in the first row does not mean there are no defects in the entire process; there are defect density assumptions throughout the baseline model to begin with. The first row only refers to zero *new* defects on top of the baseline. All results in the table are based on the assumption that an $8K wafer is being diced and placed in the package.

The table reveals clearly that the larger the package and die size, the greater the impact of the same defect density adjustment. There are two reasons for this.

First, the same level of defect density will impact differently sized packages differently. Defect density is the probability that a defect will occur in a $1cm^2$ area. The cost models assume that one defect anywhere within the package area will cause that package to be scrapped. Therefore, the larger the package, the more likely that a defect will occur somewhere within the package area.

Second, the same $8K incoming wafer is assumed in all cases. This same wafer diced into different die sizes means that a larger die costs more than a smaller die, because $8K is divided over fewer die. Therefore, larger die bring a more expensive material cost into the package, and any larger packages that must be scrapped will include the loss of that more expensive die.

B. *Die-last*

A similar analysis was carried out for die-last fan-out wafer level packaging. However, the results are more complex because they are heavily dependent on whether the defect is introduced before or after die placement. If a defect is introduced before die placement, only the cost of the processing will be lost (under the assumption that die are placed only on known good locations, due to an additional inspection step between RDL creation and die placement).

In this analysis, instead of adjusting the size of the die and package, the focus is on the change in total cost depending on whether the defect is introduced before or after die placement. The design evaluated is the 8mmx8mm package and 5mmx5mm die design from Table I. The die to be packaged come from an incoming $8K wafer, which incurs the cost of bumping in addition to the cost of dicing before being packaged.

TABLE III. DIE-LAST RESULTS

Additional defects per cm2	***Total Yield***	***% Cost Increase if defect occurs after die placement***	***% Cost Increase if defect occurs before die placement***
0.00	98.58%	0.00%	0.00%
0.02	97.36%	1.22%	0.09%
0.04	96.16%	2.41%	0.15%
0.06	94.98%	3.58%	0.21%
0.08	93.81%	4.73%	0.27%

The results show clearly that the cost increase of a defect introduced after die placement has far more impact than when that defect is discovered before die placement. The ability to potentially scrap fewer die is one of the key reasons that die-last packaging, which tends to involve more expensive processing steps, can be cost competitive with die-first processes.

V. YIELD COMPARISON

This section analyzes how the total cost of the die-first and die-last processes compare under different yield assumptions. Die-first fan-out is viewed as the more established technology, so all relative cost comparisons will be die-last compared to die-first as the baseline.

Percentages greater than 100%, indicate that the die-last package is more expensive. A red line is drawn on the charts to identify this point at which die-last packaging becomes cost-effective (when the bar drops below the red line, or 100%).

For both packaging types, the total cost takes into account:

- the processing cost.
- the cost of the incoming wafer being packaged.
- the cost of the processing being carried out on that incoming wafer
- any processing and die lost to defects as scrap.

A. *Single Die, Single RDL Packages*

The first comparison focuses on simple packages with one die and one RDL. The design details are the same as those used in the previous sections (Table I). All three designs were run for three different incoming wafer costs. The scale for each graph is the same to enable a more direct comparison between all three designs.

As stated before, when the same level of defects are assumed to be introduced in both types of processing, die-first technology will always have a higher scrap cost than die-last because the die are placed before RDL creation, a process which introduces defects. Despite this fact, the charts reveal that die-first tends to be cost-effective for packages with just one die and RDL.

The charts reveal two specific trends. First, in looking at the trend for each wafer cost (each wafer cost is the same color in each scenario), it's seen that both the $2K and $5K incoming wafers are always packaged more cost-effectively in a die-first design. The yield benefit of placing the die after RDL creation is not outweighing the greater processing and bumping costs associated with die-last processing.

Second, the charts demonstrate that the larger the package size, the greater the likelihood that die-last processing will be cost-effective. The set of bars in the final chart represent the largest package size, where the $5K bar is approaching 100% and the more expensive $8K wafer is below 100%, indicating that the die-last package is less expensive than the die-first package. This can be explained

by the earlier discussion of how the same level of defect density will more heavily impact a larger package size.

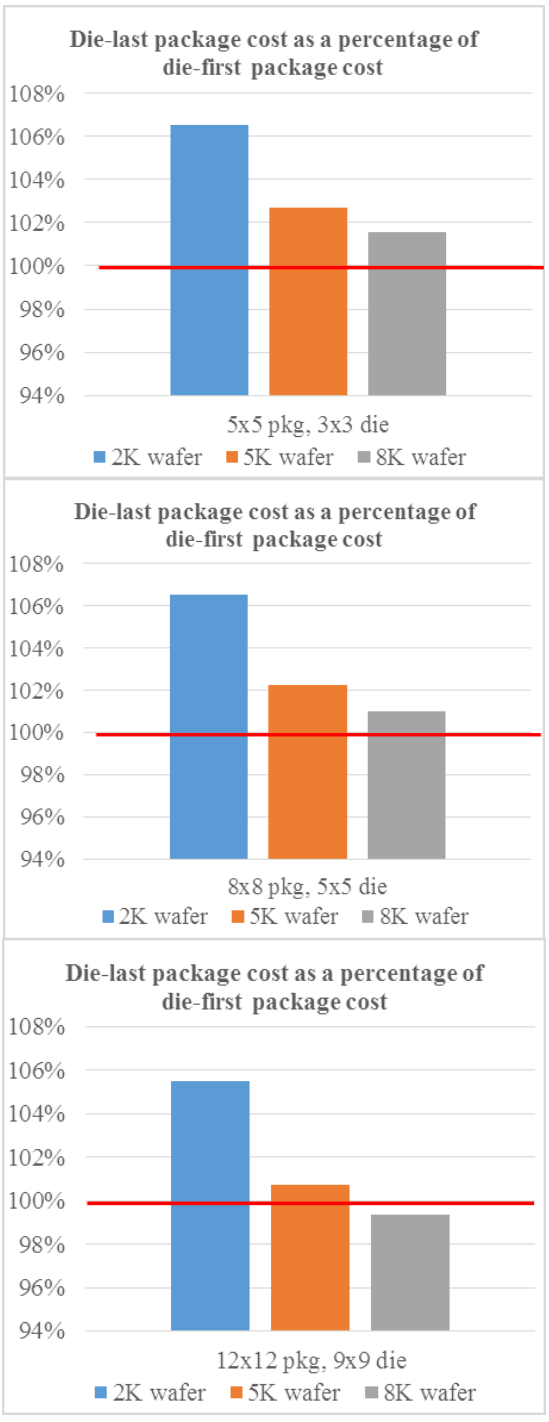

Figure 4. Yield comparison for single die, single RDL designs

B. *Multi-Die, Multi-RDL Packages*

A second round of analysis was carried out with more complex designs. A similar approach was used across a greater number of incoming wafer price points.

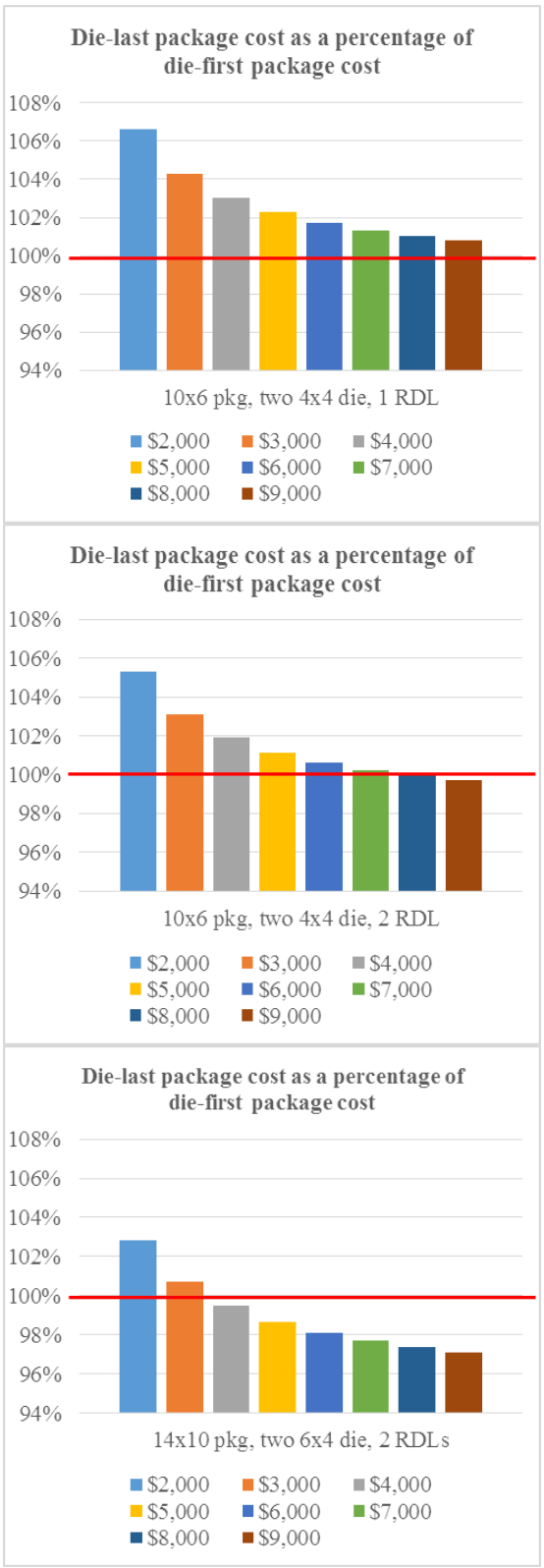

Figure 5. Yield comparison for multi-die, multi-RDL designs

The trends are similar to what was seen in the previous example with single die and single RDL designs,

but more pronounced now that more complicated designs are being analyzed. The simplest design, which is a larger package with two die but only one RDL, continues to be cost-effective as a die-first package in all cases—all of the bars in the first chart are above the red line. This is partially because the yield impact of one RDL is not very large, and partially because two die are being placed, which means the cost to bump two die is being included in the die-last processing cost.

The middle chart, which has a design with the same size and die count as the first example, but has a higher I/O count and therefore requires two RDLs, is cost-effective as a die-last design for the two most expensive wafers evaluated.

The impact of having two RDLs has created scenarios in which die-last becomes cost-effective. This is because of the impact of yield is cumulative. The fact that RDL processing introduces defects is already causing the loss of die in the die-first process, but not in the die-last process. Adding a second RDL creates cumulative yield loss, and more die-first packages are lost to scrap. The impact on the die-last process is not the same, since it has already been shown that die placed after RDL creation on a known good location in the die-last process will not suffer from defects introduced during RDL creation. The cumulative yield impact of two RDLs is moot for die-last packaging.

Despite the impact of cumulative yield creating some cases in which the die-last package is cost-effective, for the middle design, die-last is only cost-effective for the two most expensive wafers. This is because the two die being packaged are relatively small, and therefore relatively inexpensive compared to larger die coming from the same wafer. Therefore, the loss of those small die due to defects in the die-first process is not quite enough to outweigh the additional die-last costs until handling more expensive wafers.

The final package, involving two RDLs, a larger package, and larger die, becomes cost-effective quickly as a die-last package. It is more expensive to lose these large die to scrap in die-first packaging than it is to pay for the extra bumping and die-last processing costs.

CONCLUSION

Activity based cost modeling was used to compare the impact of yield on die-first face-down and die-last wafer level packaging. The cost of each process was taken into account, in addition to taking into account the yield impact of defects.

Die-first face-down processing tends to be more cost-effective than die-last fan-out wafer level packaging. Although a variety of small differences occur throughout the flows, two of the key reasons die-last processing tends to incur greater costs are the requirement for a robust temporary wafer and debond solution, and the requirement for adding bumps or copper pillars to the incoming wafer.

On the other hand, die-first face-down processing tends to be more sensitive to yield. This is due to the fact that die placement occurs early in the process, which means that any processing occurring after die placement will result in the loss of the die if that processing introduces defects.

There are many activities during both wafer level packaging processes when defects may be introduced. For the purposes of this comparison, the process flows were kept as similar as possible, and the same steps—RDL creation, die placement, and ball attach—were assumed to introduce the same level of defects in each process. RDL creation occurs before die placement in die-last processing, but after die placement in die-first processing, which means any defects introducing during RDL creation may result in the loss of die in the die-first process, but not in the die-last process.

Analysis of the individual package types revealed that the larger the die-first package, the more quickly the cost will increase as additional defects are introduced. Analysis also showed that the cost increase in die-last packaging is low when the defect occurs after die placement, but notable if it occurs after die placement.

The two package types were compared directly across a range of package types and incoming wafer costs. It was shown that die-first packaging tends to be cost-effective when dealing with single die, single RDL packages, even though the scrap cost is greater. In those cases, the additional processing costs associated with die-last packaging were not outweighed by the die-first increased scrap cost. It was only in cases when very expensive wafers were being packaged in these simpler designs that the die-last package became more cost-effective.

The results shifted when comparing larger designs with multiple die and multiple RDLs. The cumulative yield loss associated with two RDLs, and the fact that larger die-first packages are more sensitive to yield, meant that there were many cases in which die-first packaging was more cost-effective.

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