Cost Comparison of 2.5D/3D Packaging to other Packaging Technologies

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Abstract
2.5D and 3D applications using through silicon vias (TSVs) are increasingly being considered as an alternative to conventional packaging. Miniaturization and high performance product requirements are driving this move, although in many cases the cost of both 2.5D and 3D is still high.

In this paper we will identify the major cost drivers for 2.5D and 3D packaging and assess cost reduction progress, including current costs versus expected future costs. We will also compare these costs to alternative packaging.

Key words
TSV, Interposer, 3D, Cost, 2.5D

I. Introduction
When evaluating the cost of using a 2.5D or 3D solution, it is important to consider the total cost of that solution. Too often, there is a narrow focus on only one part of the cost and the total product cost is neglected [1].

Fig. 1 shows the complete flow for a 2.5D chip-on-chip process [2]. Each box in the flow has a process cost and a potential yield loss. The opportunities to test and scrap are highlighted in yellow. Note that this is only one 2.5D flow. Other flows include chip-on-substrate and chip-on-wafer. In the chip-on-substrate flow, the interposer is placed on the substrate first and then the chips are placed on the interposer. For the chip-on-wafer flow, the die are placed on the interposer before it is singulated. This has an advantage in that thin wafer handling problems are minimized because the addition of the active die adds stability to the interposer wafer before it is thinned.

Figure 2 shows a complete flow for a 3D chip-on-chip process. While there are just as many opportunities in the 3D flow to test and scrap, it is important to note that 100% test coverage is not always possible. This means the yield coming out of the test and scrap activity may not be 100%, and any defects that escape the test will cause a failure later in the process flow. Interposers and substrates are easier to fully test than active die, and are therefore less likely to contain fatal defects that pass the wafer testing. Due to this fact, the 2.5D flows will generally have a higher cumulative yield at final test compared to a full 3D flow.

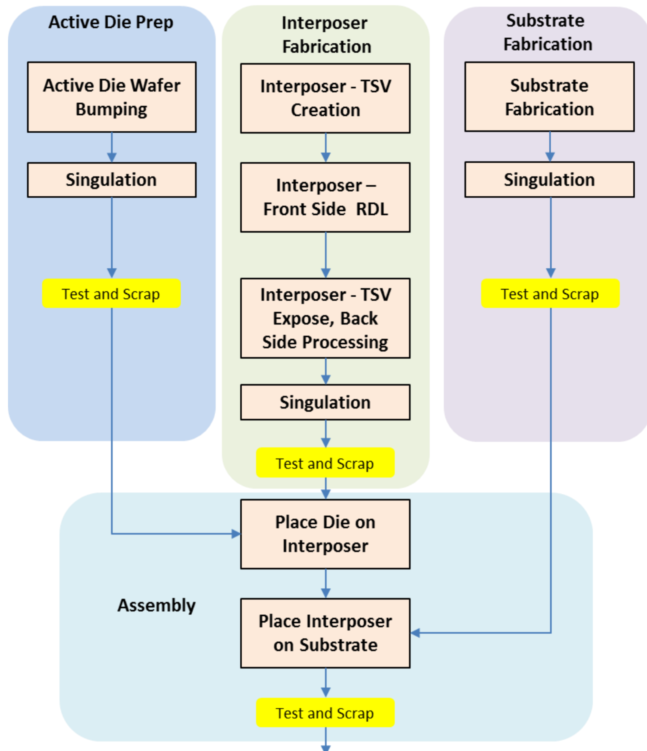

Figure 1 – 2.5D Chip-on-Chip Process Flow

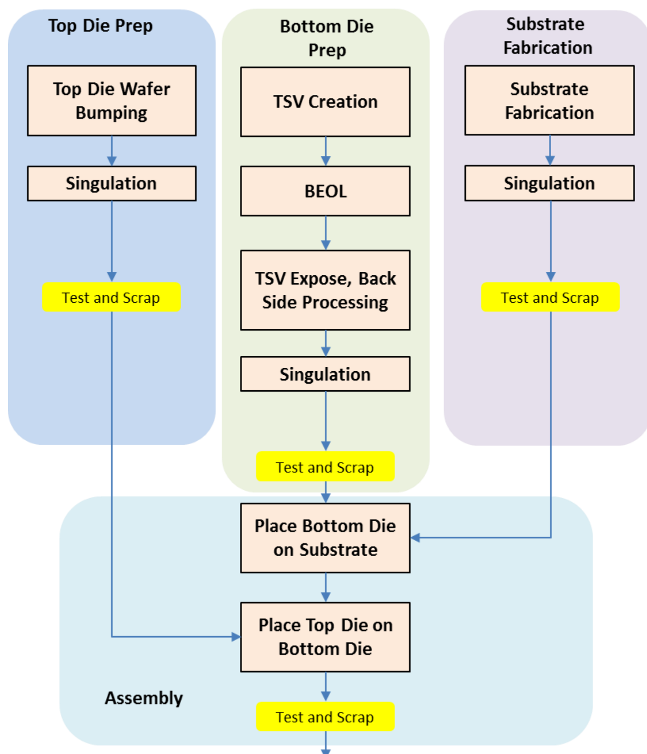

Figure 2 – 3D Chip-on-Chip Process Flow

II. 2.5D and 3D Cost Drivers

The cost drivers for 2.5D and 3D manufacturing flows can be divided into the following three categories.

- Direct Process Costs – These include the measured labor, equipment depreciation, and material costs for each step in the manufacturing process.
- Yield Loss – Any defects that are either introduced or discovered during the manufacturing process will add cost. In most cases defects cause scrap, but in some cases rework may be possible.
- Indirect, Overhead, and Liability Risk Costs – These costs are not as easily measured as the first two categories. They are typically applied as a percentage of the direct costs.

A. Direct Process Costs

Process costs are the easiest to measure and therefore usually attract the most attention. While 2.5D and 3D technologies are new, it is important to note that most of the activities required for this technology are not new and therefore may not decrease in cost over time. Activities including wafer bumping, die bonding, substrate fabrication and final assembly are currently part of most modern flip chip process flows and are mature, stable processes. Below is a list of the dominant direct process cost drivers that are specific to TSVs.

- TSV Creation – TSV creation must be done in a fab environment in a class 10 or better cleanroom with relatively expensive equipment associated with the semiconductor fabrication process. The individual activities in this flow—PVD (physical vapor deposition), CVD (chemical vapor deposition), DRIE (deep reactive-ion etch), CMP (chemical mechanical planarization), and electroplating to fill the vias—are commonly found in a fab operation.
- TSV Expose and back side processing – This process is a significant cost driver given the slow throughput and challenge of thin wafer handling.
- Front side RDL on interposer or active die – This is a common activity for a fab and may also be done by an OSAT if fine line and spacing is not required. It can either be done as a dual damascene semiconductor process if fine lines and spacing are required, or as an RDL similar to a wafer level packaging process.

B. Yield Loss

Yield loss is an important and frequently overlooked cost driver for new technologies. The flows in Fig. 1 and 2 show the various opportunities for test and scrap. Below are the details of each of these test and scrap steps.

- 2.5D active die prep or 3D top die prep after singulation – This is typically a wafer probe of a normal active die. However, not all defects will be detected during a typical wafer probe process. If this die were destined to be packaged in a normal flip chip or wire bond process, final burn-in testing would be used to detect bad die that wafer probe missed.
- 2.5D Interposer fabrication after singulation – Since an interposer typically does not contain active devices, open/short testing may be sufficient and should result in fewer defects that escape the testing process.
- 3D bottom die prep after singulation – This is a test of an active die plus TSVs. This is a difficult test to accomplish thoroughly and accurately given the range and complexity of potential defects. It is also quite important, since any defect escapes will cause a very expensive scrap at the end of the process.
- 2.5D/3D substrate fabrication after singulation – This is a straight forward test done successfully today. In a typical packaging flow today, most failures found after the die is placed on the substrate are usually undetected die defects, not substrate fabrication or assembly defects.
- 2.5D/3D final test and scrap – This is a thorough test of the complete package, interposer, and all die, and it is done much the same way as burn-in testing is done in a traditional packaging flow. Any defects found during this test cause a scrap of everything—interposer, all die, and the substrate.

C. Indirect, Overhead, and Liability Concern Costs

One of the largest cost components of 2.5D and 3D products are indirect, overhead, and liability concern costs. The total direct cost for a 2.5D silicon wafer has been reported to be around $600 [3]. However, the total process of an interposer has been quoted to be between $2000 and $3000 [4]. While margin is responsible for some of the difference between direct cost and price, other significant components are indirect costs, overhead, and a liability risk factor. The overhead costs associated with activities done in a semiconductor fab will be much higher than the overhead for activities done at a substrate fabricator or an OSAT. Overhead costs include the cost to build and operate the factory, and these are much higher for a semiconductor fab than for a factory that manufactures or assembles organic substrates.

2.5D and 3D flows disrupt the supply chain, which means that bare die or partially processed interposers may be sent between suppliers. Furthermore, die from different suppliers may be placed on the same interposer. If a defect is found at the end of the process, the question inevitably asked is: who pays? [5] In order to compensate for these risks and liability concerns, the prices being charged for 2.5D and 3D products and services are higher than the direct costs would indicate.

III. Sensitivity Analysis of Yield

One of the reasons product design groups consider 2.5D instead of 3D technology is because 2.5D flows limit the cost impact of low yields for the TSV creation process. In 3D designs, the TSVs are created during the fabrication of the active silicon. Therefore, the yield loss from TSV creation will compound the yield loss of the active silicon. The cost disadvantage of 2.5D, on the other hand, is the addition of an interposer to the package. Alternative packaging approaches including flip chip, wire bond, and 3D do not require an interposer between the active silicon die and the organic substrate.

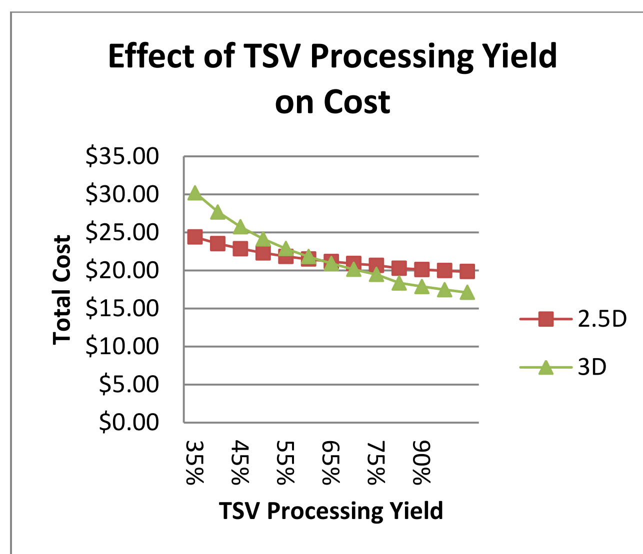

Figure 3 – TSV Processing Yield Effect on Cost

The graph in Fig. 3 shows the cost impact of TSV processing yield on 2.5D and 3D designs for a 2 die example. Each die is 10x10mm; they are stacked for the 3D case and placed side by side on an interposer for the 2.5D case.

If the TSV processing yield is low, the 2.5D technology has a cost advantage over 3D. The reason is that the TSVs are in an interposer, so only the interposer must be scrapped if

the yield is low. However, if the TSVs are added to the active die, as in the 3D case, expensive active die will be scrapped if there are TSV failures. Conversely, if the TSV processing yield is high, 3D technology has a cost advantage over 2.5D technology because 3D technology does not require an interposer.

IV. 2.5D and 3D Comparison to Other Technology

The example below is a comparison of 3D stacked die technology, fan-out wafer level packaging (FOWLP) for package on package (PoP), and traditional packaging for PoP. For the traditional packaging PoP, the bottom package is a flip chip and the top package is a wire bond PBGA.

Table I – Baseline Assumptions

Assumptions - Baseline Case	
DRAM Wafer Cost	$4,000
Logic Wafer Cost	$5,000
Burn-in Yield Loss	5%
3D process yield	75%
FOWLP process yield	90%
FC & WB assembly yield	99%

For the baseline case, we calculate the total cost including silicon, packaging, and scrap for 2 10x10mm die—one logic and one DRAM. Table II below shows the total cost of the three technologies. As expected, the cost for traditional PoP packaging is the lowest cost. However, even though all three of these technologies involve placement of a die above another die, traditional PoP and FOWLP PoP will only support a small number of die to die signals, and the performance of these signals will be limited.

Table II – Baseline Case Total Cost

Total Cost - Baseline Case	
3D	$21.72
FOWLP PoP	$18.30
Traditional Packaging PoP	$15.15

While the processing yield for both FOWLP PoP and full 3D are low today, it is reasonable to expect that these yields will improve over time. Tables III and IV show the same case with improved yields. The lowest cost option is still traditional packaging, but if the product requirements necessitate high bandwidth and high performance between the 2 die, a 3D solution may be the lowest cost option to meet these requirements.

Table III – Improved Yield Assumptions

Assumptions - Improved Yield	
DRAM Wafer Cost	$4,000
Logic Wafer Cost	$5,000
Burn in Yield Loss	3%
3D process yield	95%
FOWLP process yield	95%
FC & WB assembly yield	99%

Table IV – Improved Yield Case Total Cost

Total Cost - Improved Yield	
3D	$16.45
FOWLP PoP	$16.98
Traditional Packaging PoP	$14.84

V. Summary / Conclusion

In summary, there are three key points regarding 2.5D and 3D costs.

- Analyzing only the direct process costs of 2.5D and 3D manufacturing activities is inadequate for making the right technology decision. Yield loss throughout the complete manufacturing flow and all indirect, overhead, and risk factor costs must be considered.
- 2.5D technology can be used to isolate the yield loss associated with TSV creation. If this yield loss is high, 2.5D may have a cost advantage over 3D even though 2.5D requires a fully processed interposer. Once the TSV processing yields are high, 3D will have a cost advantage.
- Even with high yields, it is unlikely that 3D will cost less than traditional packaging, PoP or otherwise. However, traditional packaging may be insufficient to support product requirements involving a large number of die to die signals and high performance.

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