Cost Comparison of Fan-out Wafer Level Packaging and Flip Chip Packaging

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Agenda

➢ **Introduction**

➢ **Process Flows**
- Flip Chip
- Fan-out Wafer Level Processing
- Yield Differences

➢ **Activity Based Cost Modeling**

➢ **Cost Comparison**

➢ **Summary**

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➢ **Fan-out technology and flip chip technology are suitable for many of the same applications**

- Flip chip is more mature
- Advancements are occurring in both

➢ **The right packaging choice is the one that meets design requirements at the lowest cost**

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Process Flows

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➢ **Three segments to the process flow**

- Wafer preparation - Includes the addition of bumps or copper pillars, dicing, and thinning if necessary
- Substrate fabrication
- Assembly

➢ **Typical process flow on next page**

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Typical Flip Chip Process Flow

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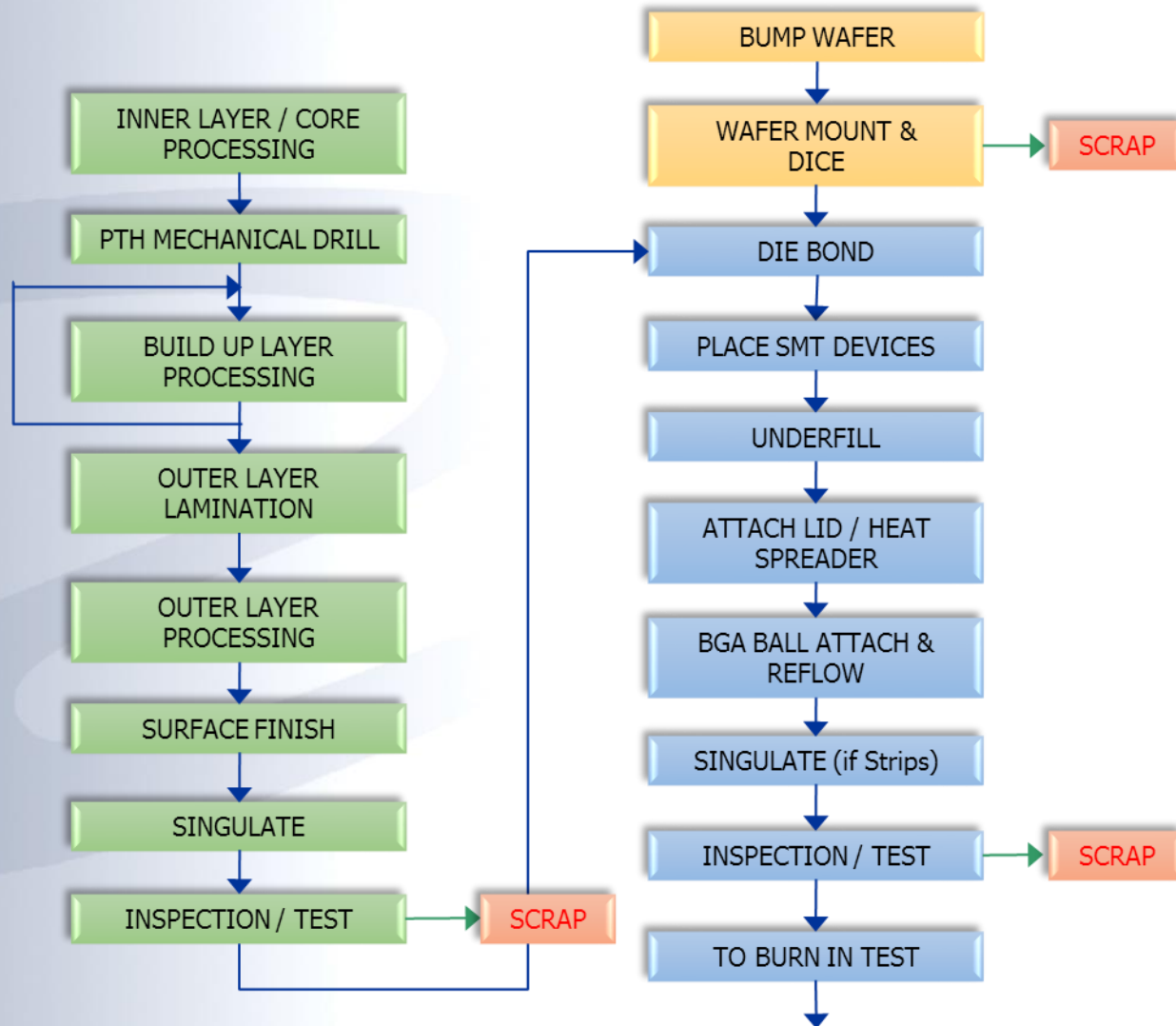
Fan-out Wafer Level Packaging

➢ **Die-first (face down) selected for analysis**
- Other variations exist

➢ **Two segments to the process flow**
- Wafer preparation – Includes dicing, and thinning if necessary
- Substrate and assembly are basically combined

➢ **Typical process flow on next page**

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Typical Die-first (face down) Process Flow

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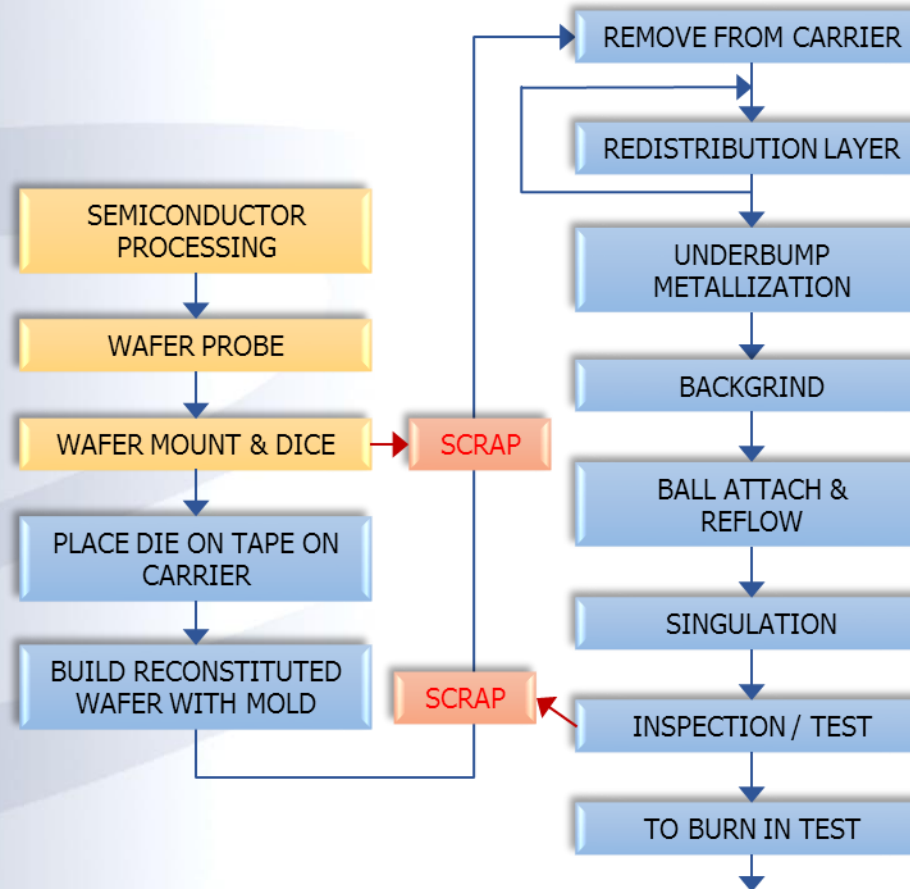
Yield Differences

➢ **Of the many differences between the flows, yield is key**

- Major impact on the cost comparison

➢ **Scrap points**

- Three during flip chip processing
- Two during fan-out WLP processing

➢ **Analysis will take into account:**

- Cost of processing (including wafer preparation)
- Cost of the incoming die
- Cost of processing lost to scrap
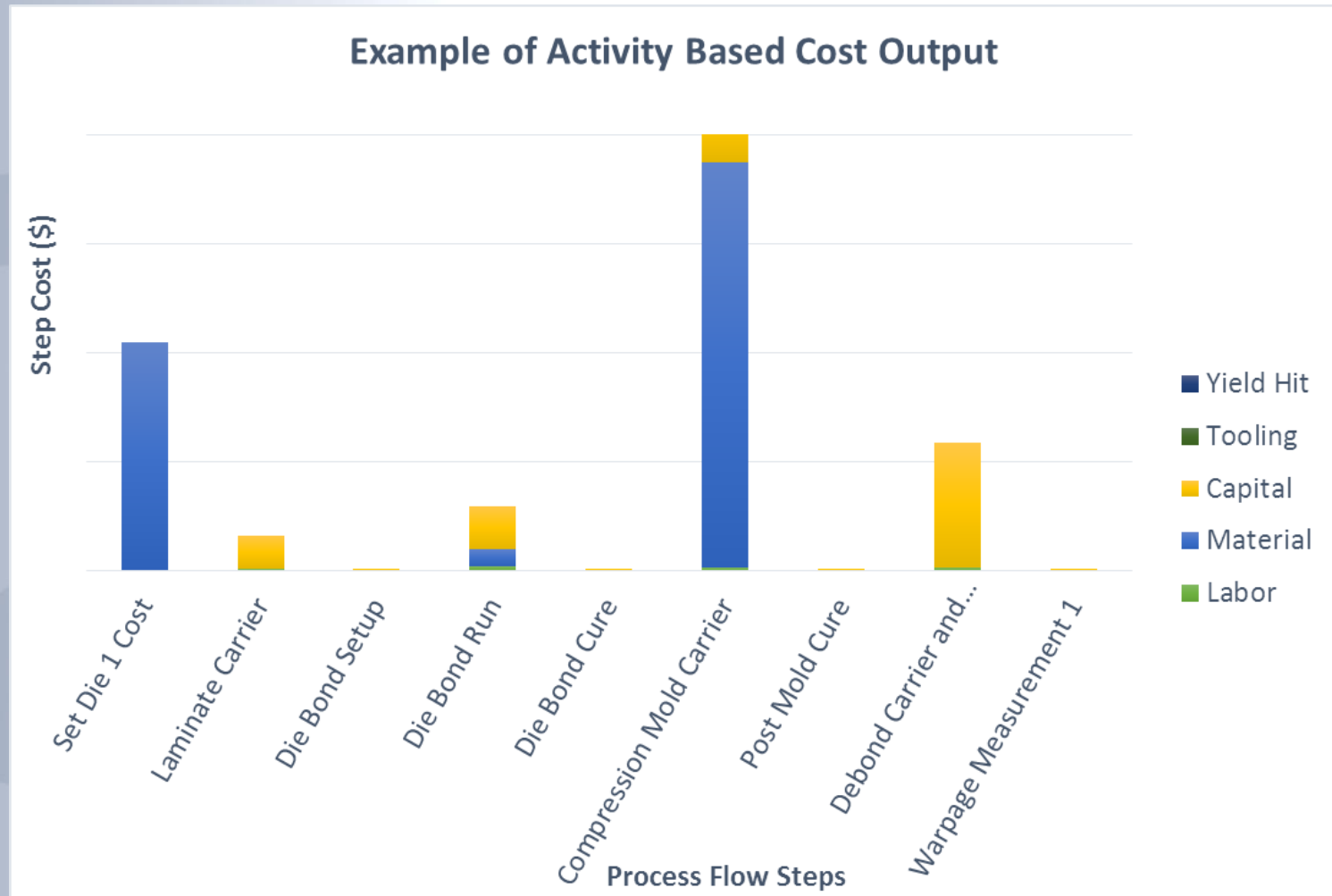- Cost of die lost to scrap

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Activity Based Cost Modeling

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Activity Based Cost Modeling

➢ **Cost Components of each Activity**

- The time required to complete the activity
- The amount of labor dedicated to the activity
- The cost of material required to perform that activity – both consumable and permanent material
- Any tooling cost
- All capital costs associated with the equipment required to perform the activity
- The yield loss associated with the activity

➢ **Sample Output**

Substrate	Labor	Material	Capital	Tooling	Yield	Macro	Running Total
2-[IL-Core]	$0.0007	$0.2000	$0.0007	$0.0000	$0.0000	$0.0000	$0.2014
3-[IL-Photoresist]	$0.0007	$0.0120	$0.0011	$0.0000	$0.0000	$0.0000	$0.2152
4-[IL - Image]	$0.0007	$0.0144	$0.0045	$0.0000	$0.0000	$0.0000	$0.2349
5-[IL-DES]	$0.0009	$0.0072	$0.0088	$0.0000	$0.0000	$0.0000	$0.2517
6-[IL - Oxide]	$0.0010	$0.0001	$0.0026	$0.0000	$0.0000	$0.0000	$0.2554
7-[IL-AOI]-[Setup]	$0.0001	$0.0000	$0.0006	$0.0000	$0.0000	$0.0000	$0.2561
7-[IL-AOI]-[Test]	$0.0025	$0.0000	$0.0099	$0.0000	$0.0000	$0.0000	$0.2686

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Example of Activity Based Cost Output

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Component	Description
Direct Cost	Measured Cost – May be done at the activity level or at the factory level
Indirect Cost	Factory cost that is not directly associated with an activity. Support, quality, manufacturing engineering, utilities, plant, etc.
Overhead	Company cost that needs to covered. Typically G&A, marketing, engineering, etc.
Profit Margin	Usually a percentage on total cost
Risk Factor	A higher than usual margin allocated to new technologies

Cost models are used to estimate this directly

While all 4 of These vary widely, their total is driven to a level of consistency by the market. They are usually applied on top of direct cost as a % and per manufacturing object

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Cost Comparison

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➢ **Many design details impact the cost of a design**

  • Package size, die size, I/O count, substrate structure (flip chip), etc.

➢ **Different design features isolated through comparisons to highlight impact of a single feature**

  • Look for trends
  • Real world comparisons would typically involve more than a single design detail being adjusted

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> ## Same die is placed in different package sizes

- I/O count is driven by package size, so I/O count is adjusted for each design
- Processing costs (and processing scrap) only

Varying pkg size for 5x5mm die - Processing Costs

Varying pkg size for 3x3mm die - Processing Costs

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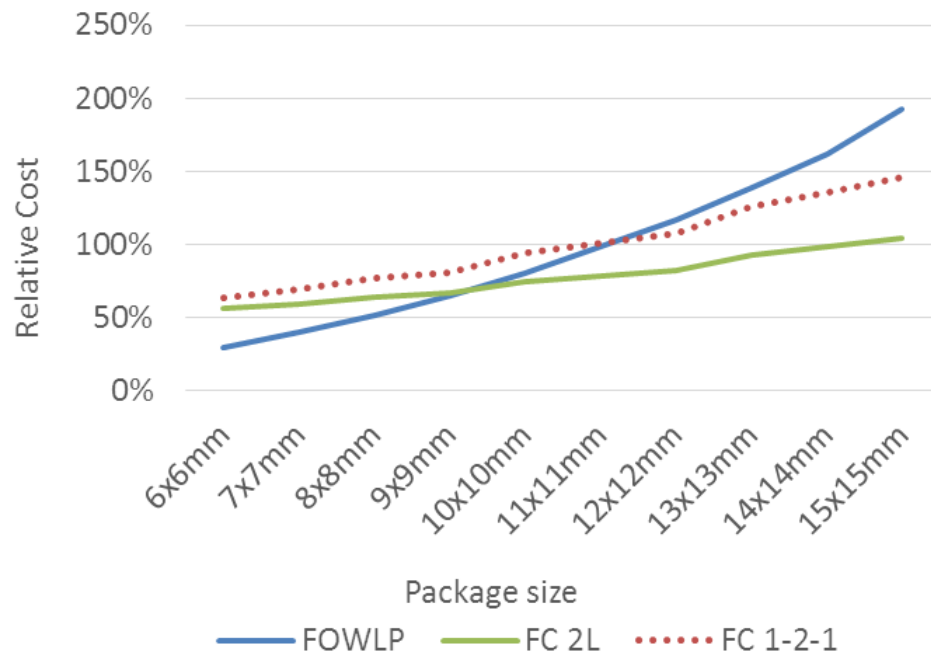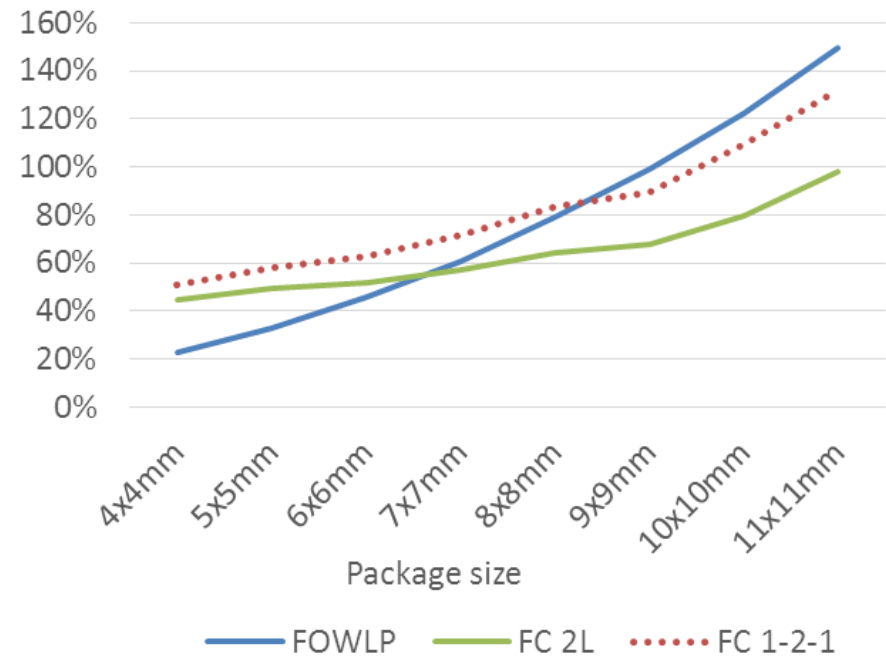
Overall, the larger the package size, the more likely flip chip processing will be cost-effective

Varying pkg size for 5x5mm die - Processing Costs

Varying pkg size for 3x3mm die - Processing Costs

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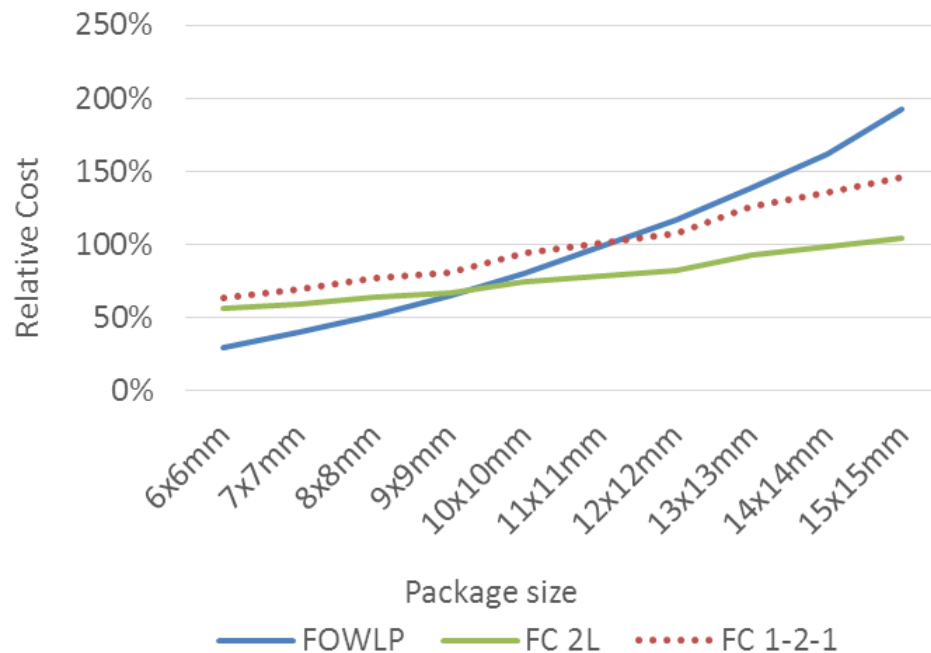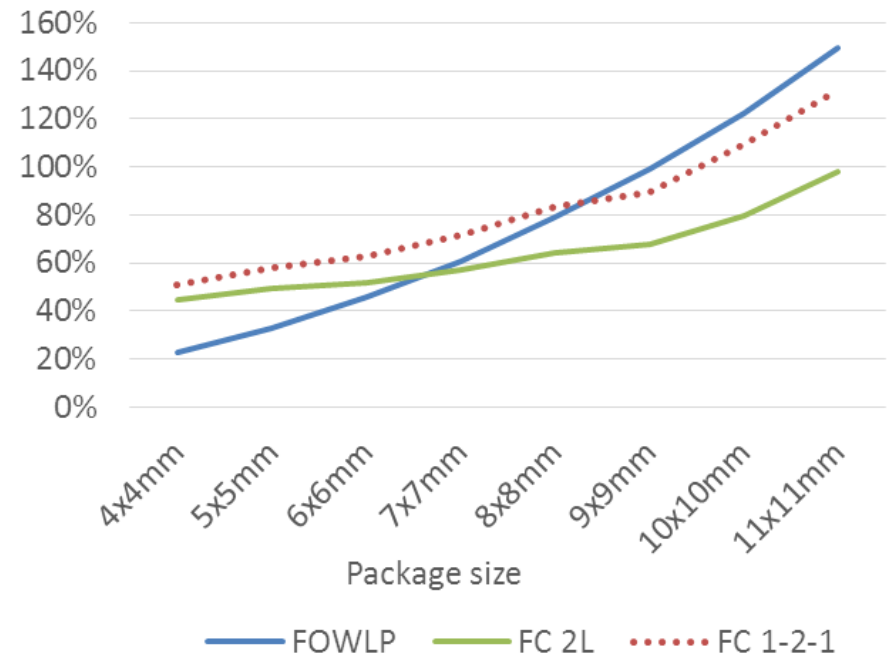
FOWLP no longer cost-effective at 9x9mm for larger die, but the crossover happens ~6x6mm for the smaller die

Size of the package in relation to the die has an impact → In FOWLP, the smaller the package in relation to the die, the less mold required, which results in lower processing costs

Varying pkg size for 5x5mm die - Processing Costs

Varying pkg size for 3x3mm die - Processing Costs

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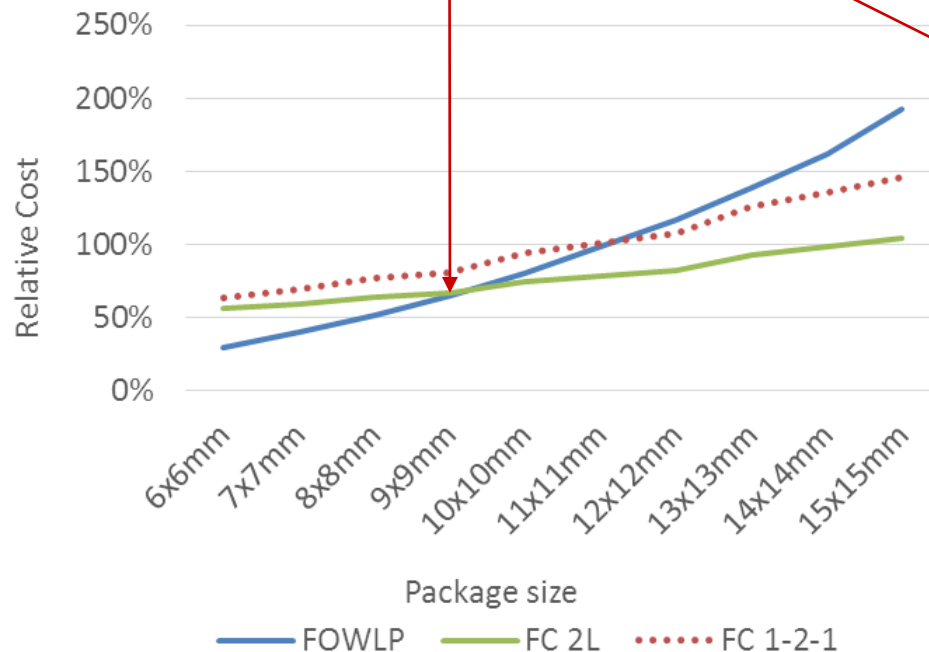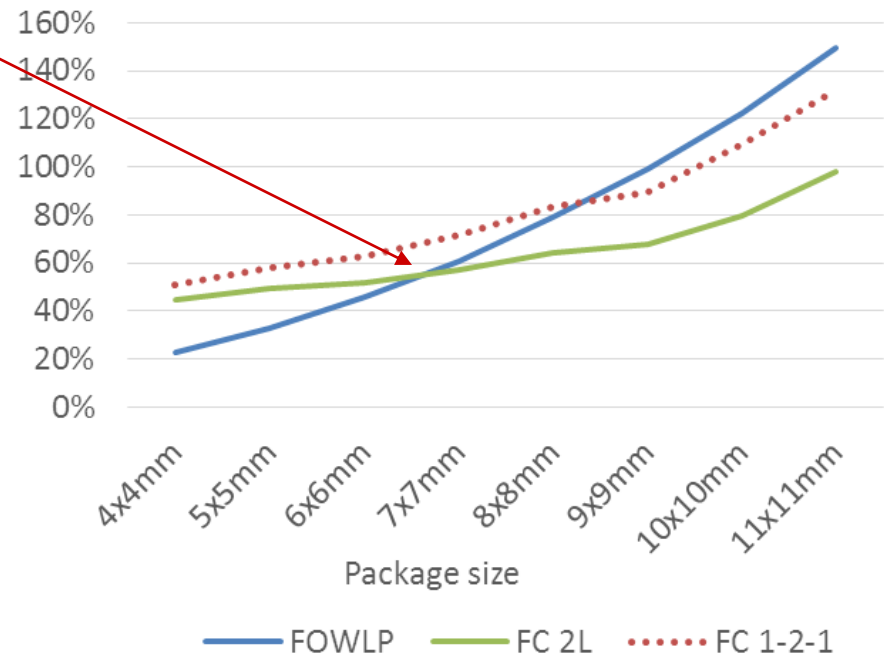
FOWLP cost is heavily driven by package size → Steeper slope
Many FOWLP activities are performed on the entire wafer at once, so the same cost
is spread out over fewer packages as package size increases
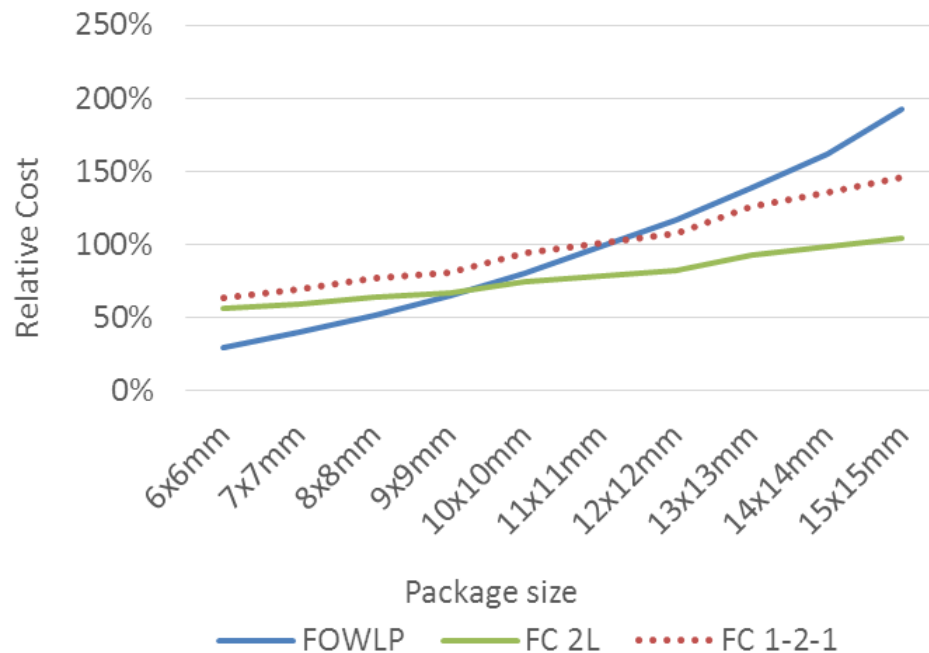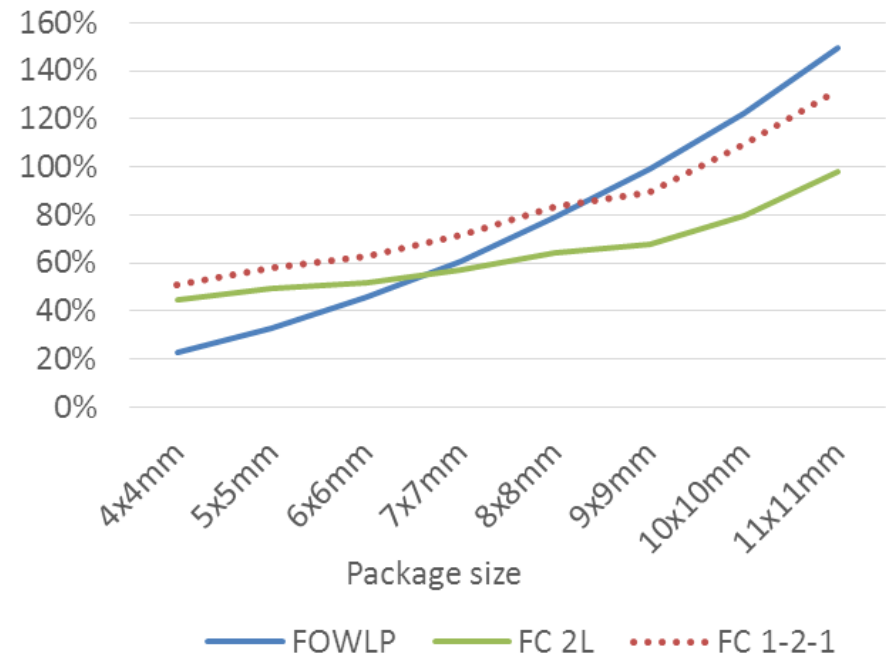
Varying Package Size

Flip chip is less sensitive to increasing package size → Slope isn't as steep
Die preparation cost is static, and it doesn't change with package size

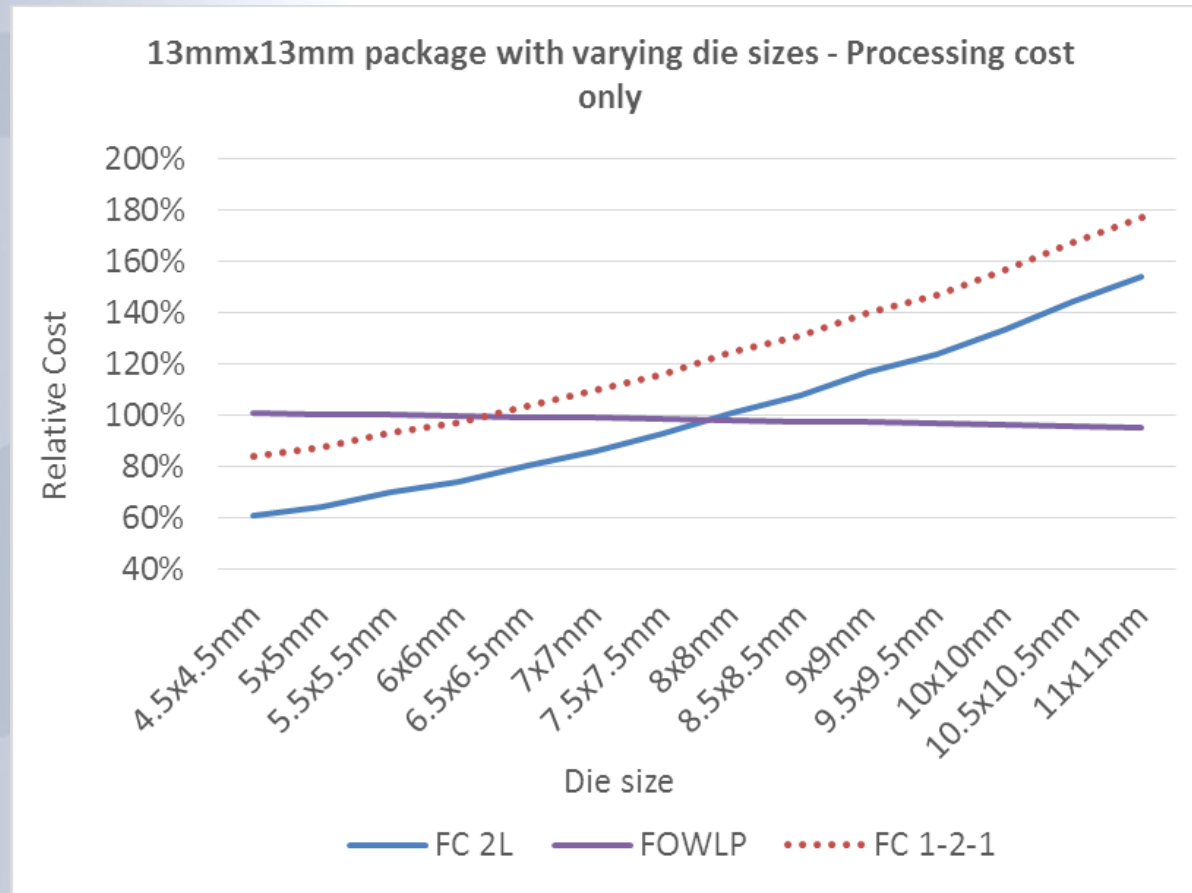Varying pkg size for 5x5mm die - Processing Costs

Varying pkg size for 3x3mm die - Processing Costs

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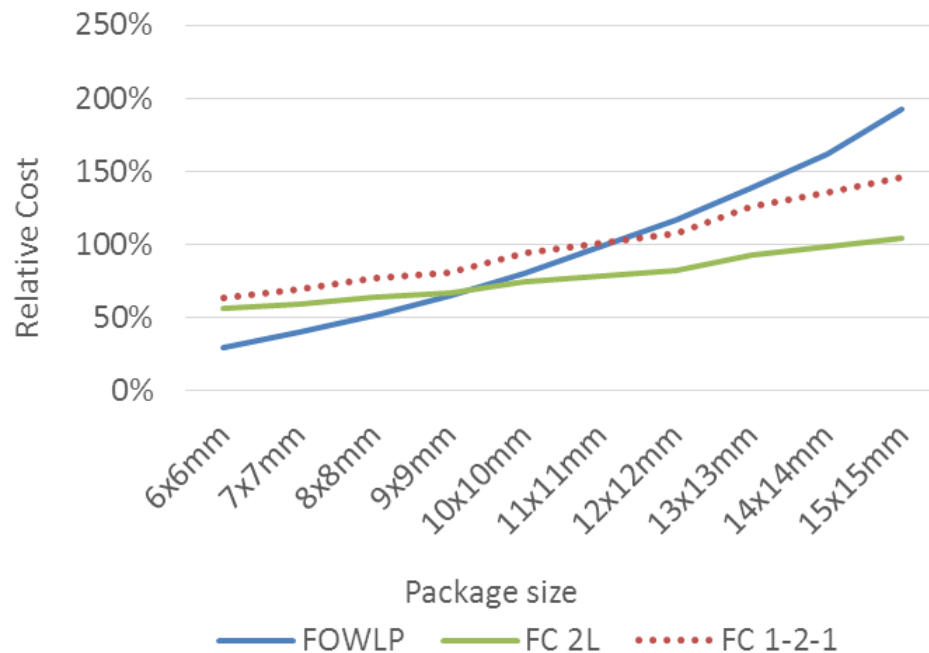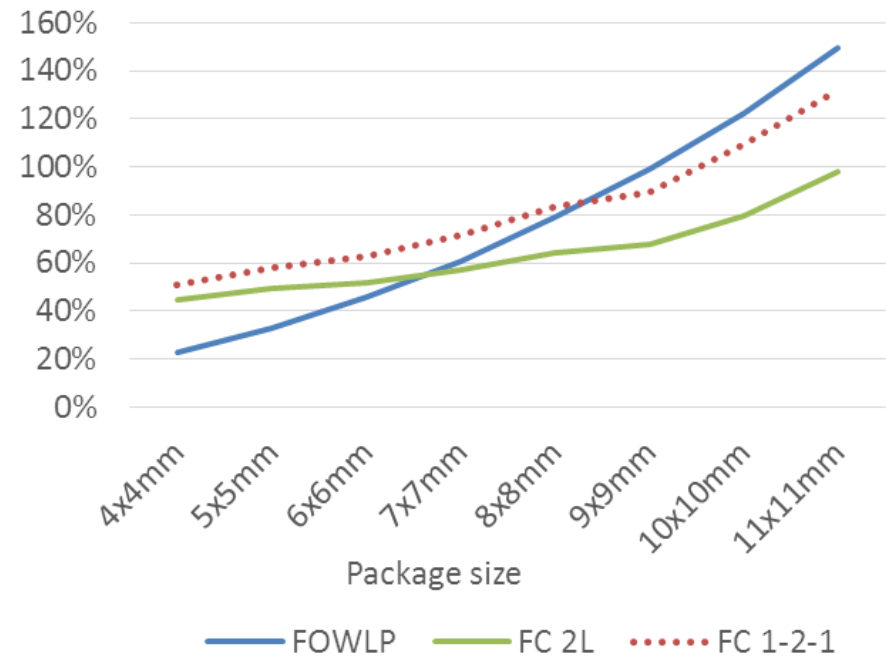
➢ **Package size is constant, die size is adjusted**

- Processing costs (and processing scrap) only

13mmx13mm package with varying die sizes - Processing cost only

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FOWLP cost is nearly static, since it largely depends on package size → Cost actually goes down at larger die sizes because less mold is required

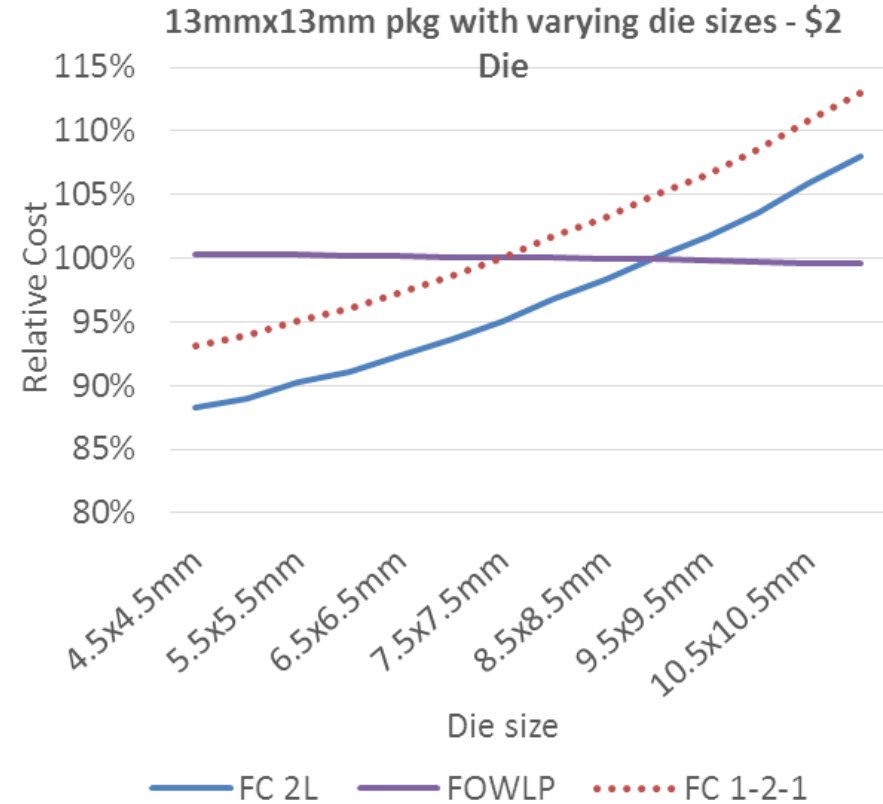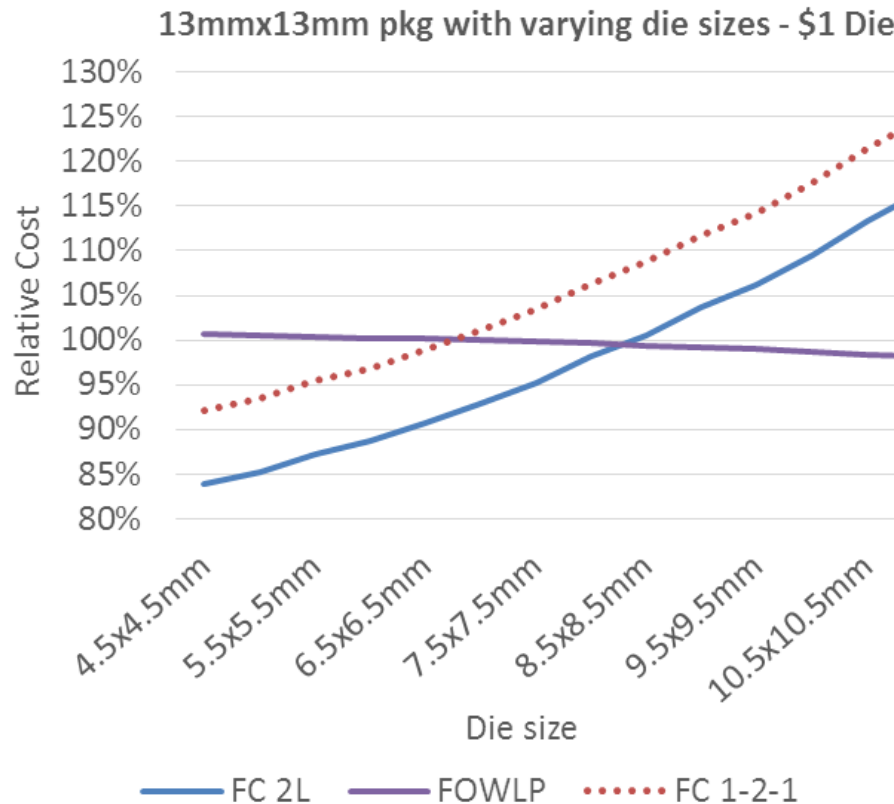Flip chip cost changes primarily because a large die brings in a larger processing (wafer bumping) cost

13mmx13mm package with varying die sizes - Processing cost only
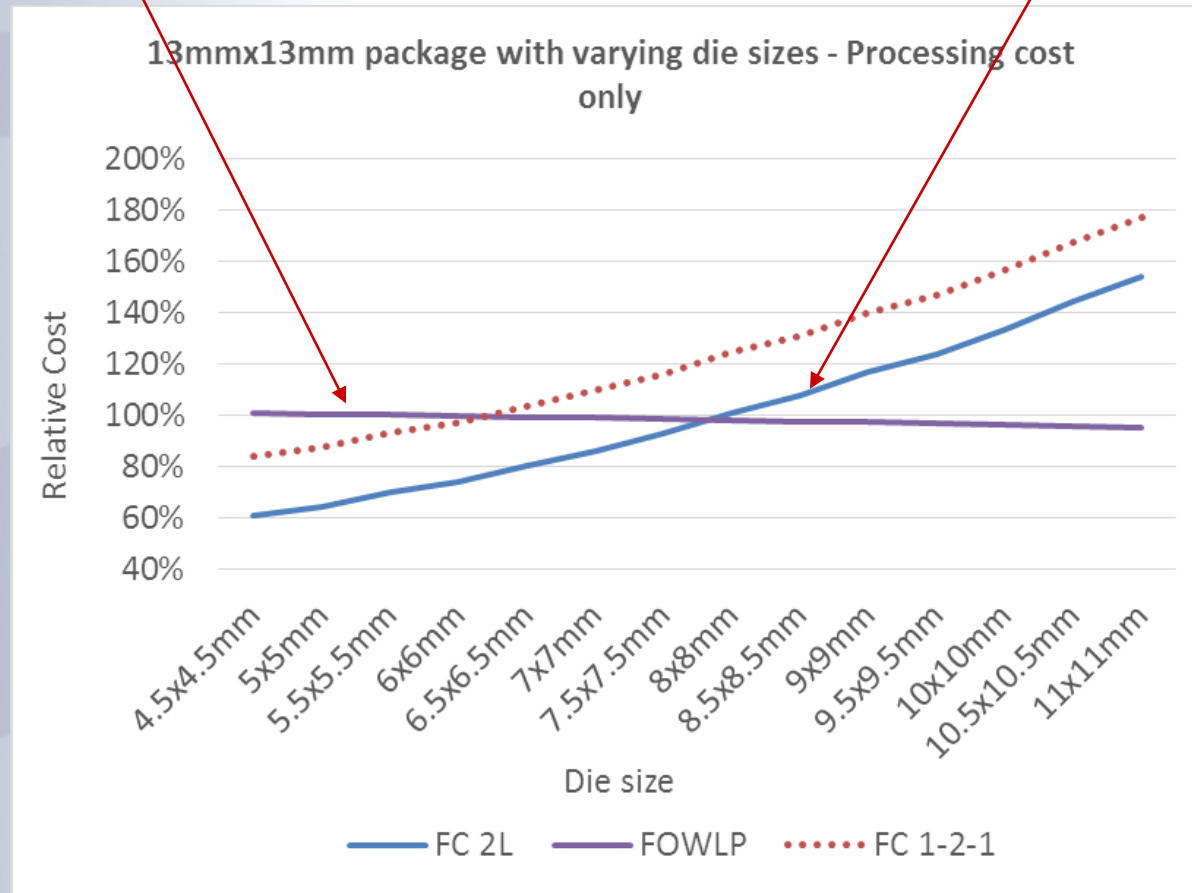
Flip chip cost is heavily impacted by die size changes → The larger the die, the greater the cost from bumping the wafer, and the less likely it will be cost competitive with a similar fan-out design

13mmx13mm package with varying die sizes - Processing cost only
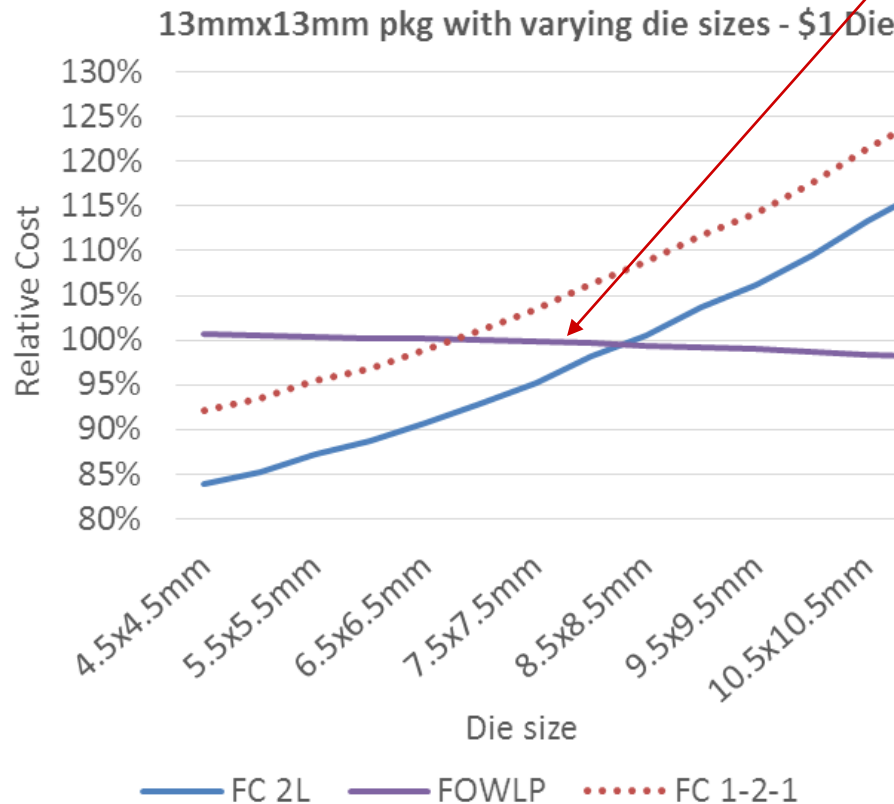
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> **Same example, but die cost and die scrap are included**

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When only processing cost was taken into account, crossover was around 7.5x7.5mm

13mmx13mm pkg with varying die sizes - $1 Die

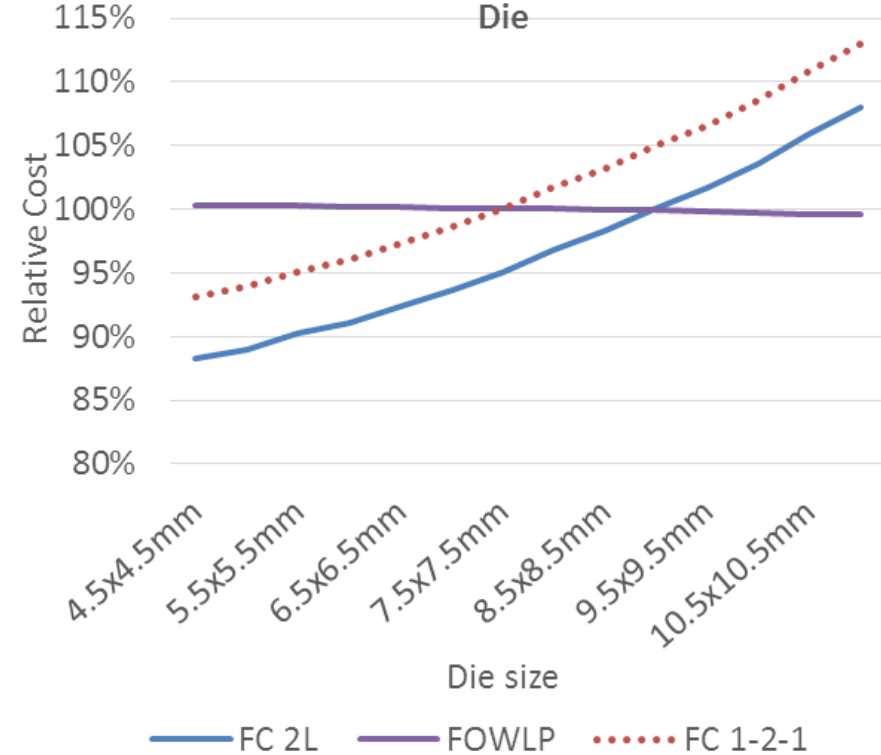13mmx13mm pkg with varying die sizes - $2 Die

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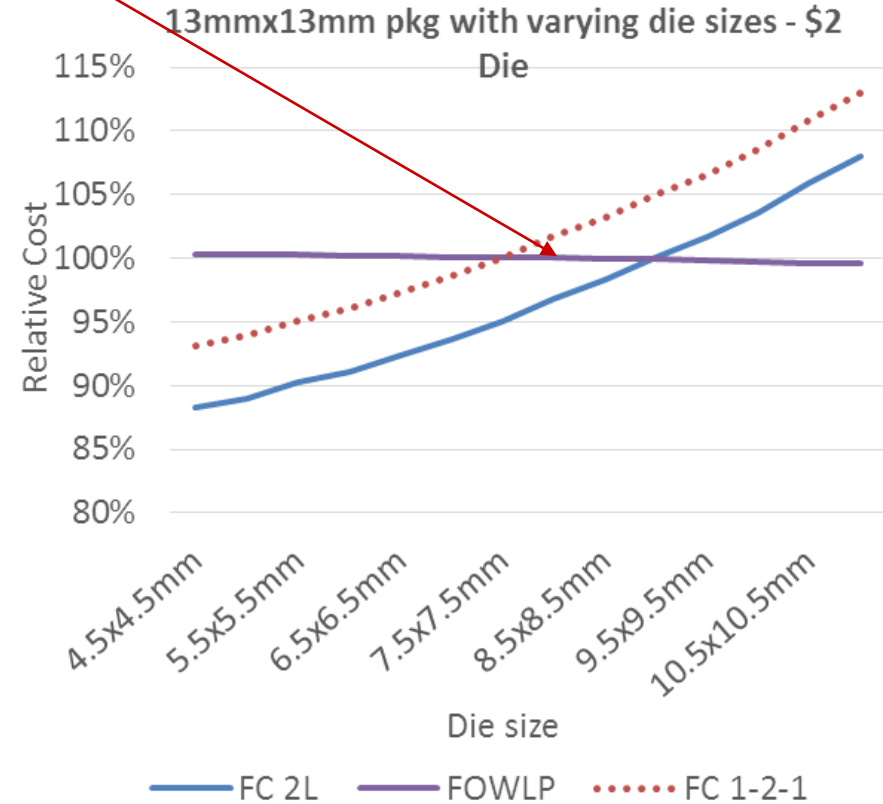
Varying Die Size – With Die Cost

The more expensive the die being packaged, the higher the potential scrap cost of FOWLP

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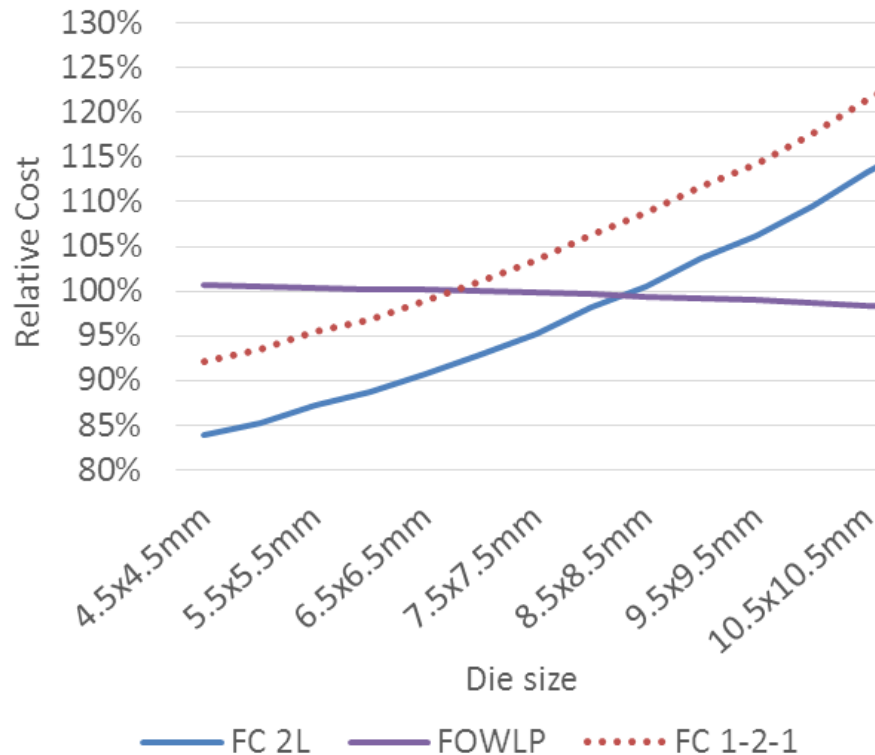
➢ **Previous example showed crossover point shifting based on processing cost versus total cost**

- Flip chip packaging cost-effective in more scenarios when cost of a die + scrap taken into account

➢ **Fan-out WLP more sensitive to yield**

➢ **Cost models use defect density assumptions**

- Defect density is the probability that a defect will occur in a $1cm^2$ area
- Models assume one defect anywhere within the package area will cause that package to be scrapped
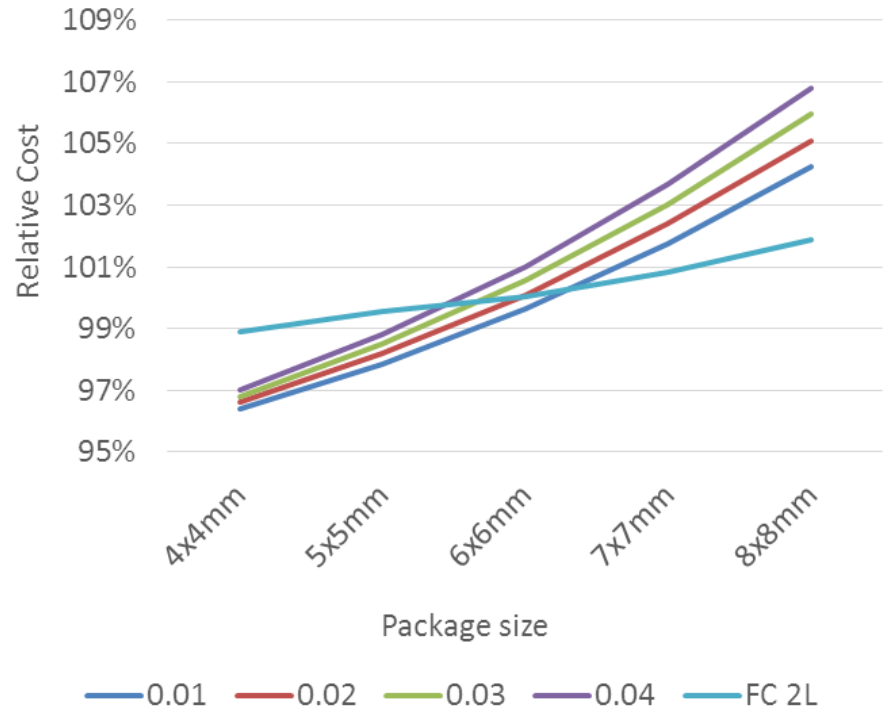
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Yield Analysis – Varying Package Size

Total yield for 0.01 defect density line is ~99.5%, yield for 0.02 line is ~99%*
FC yield is also in the high-nineties

*Many current fan-out processes have yields higher than 99%. The options in the graph were selected to show the impact of yield. More complex packages and newer FOWLP technologies will have yields lower than 99%.

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FC becomes cost-effective from a ~6x6mm package vs. the lowest yield FOWLP example

FC becomes cost-effective for a ~6.5x6.5mm package vs. the FOWLP process with the best yield

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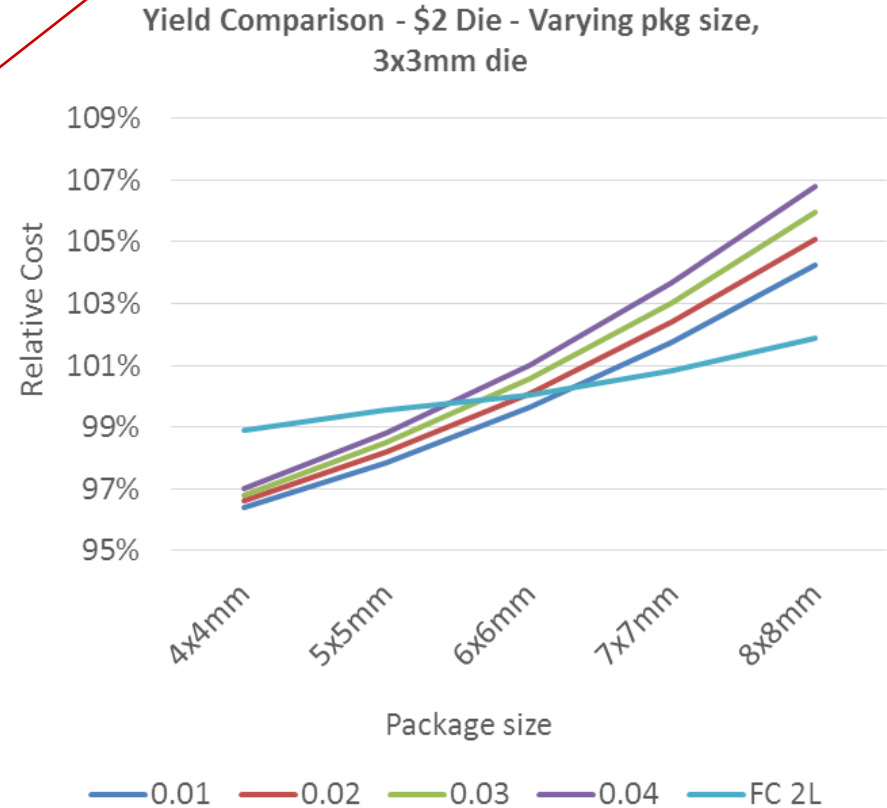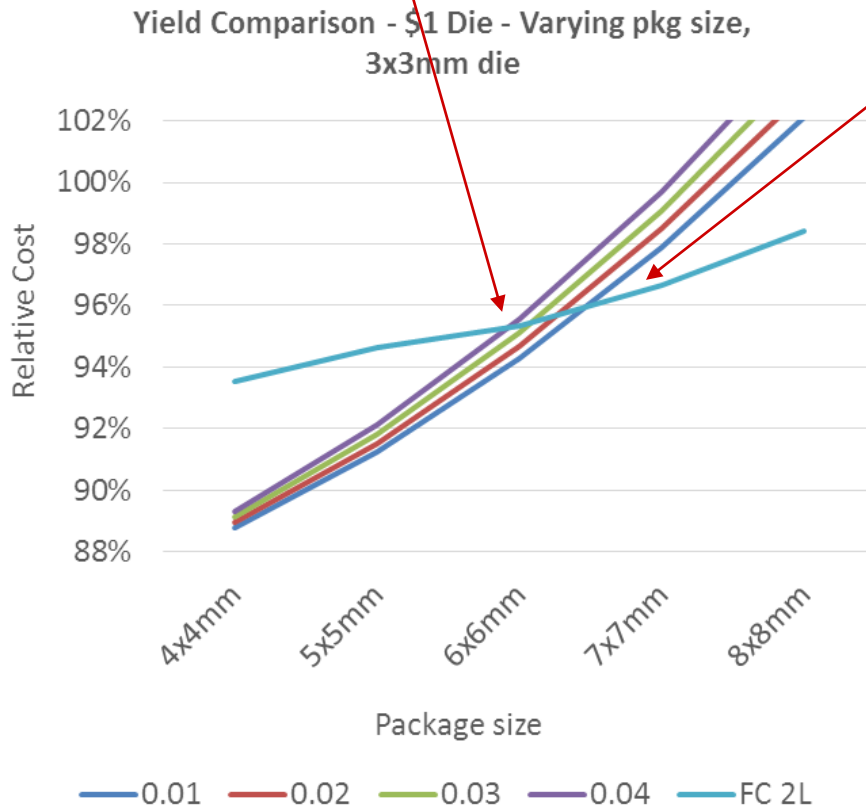
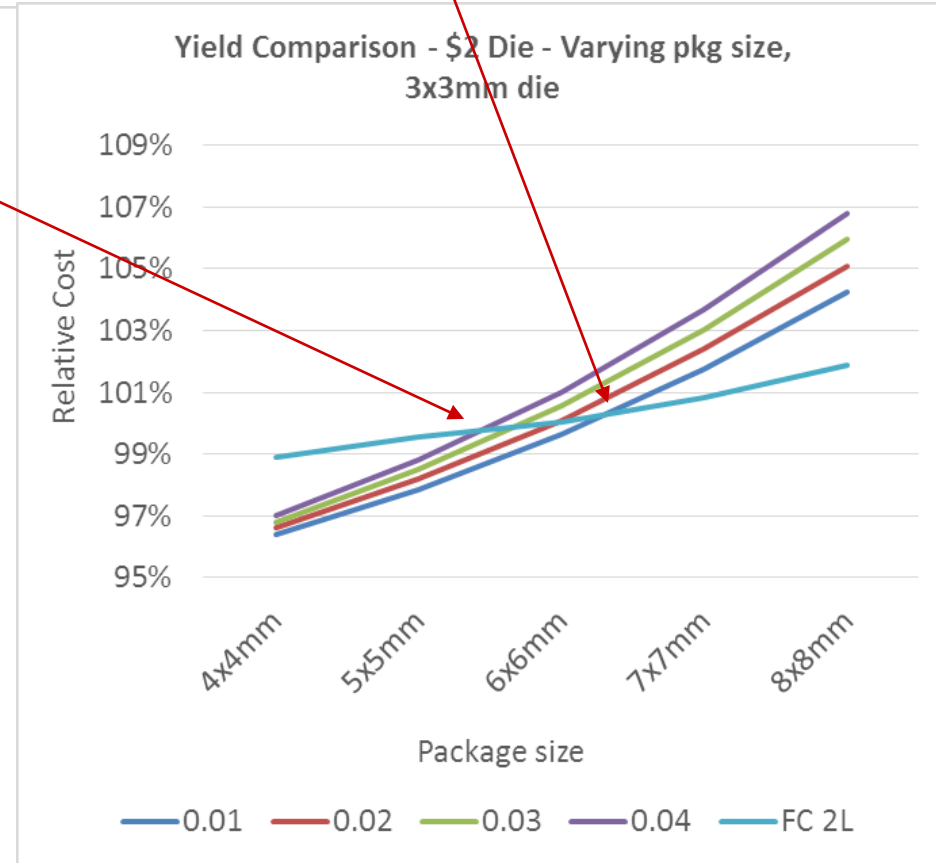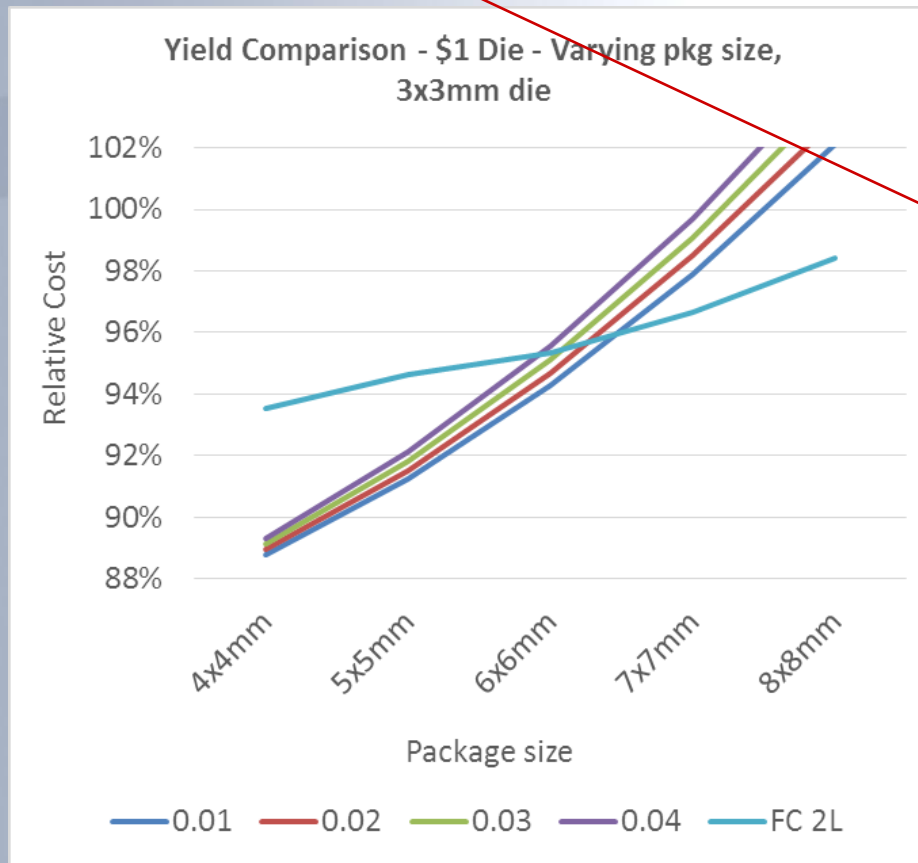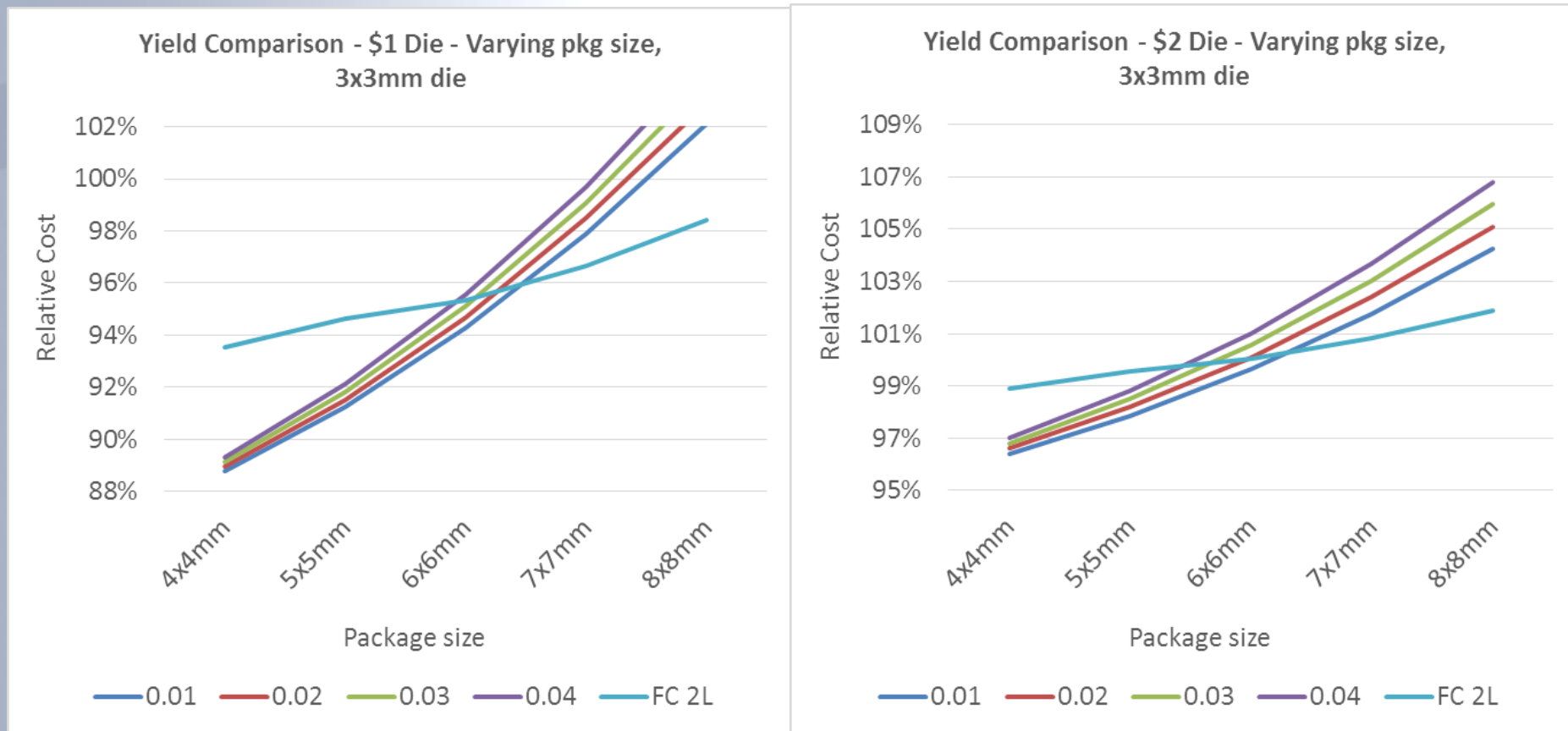FC becomes cost-effective for a 5.5x5.5mm package vs. the lowest yield FOWLP example

FC becomes cost-effective for a 6.5x6.5mm package vs. the FOWLP process with the best yield
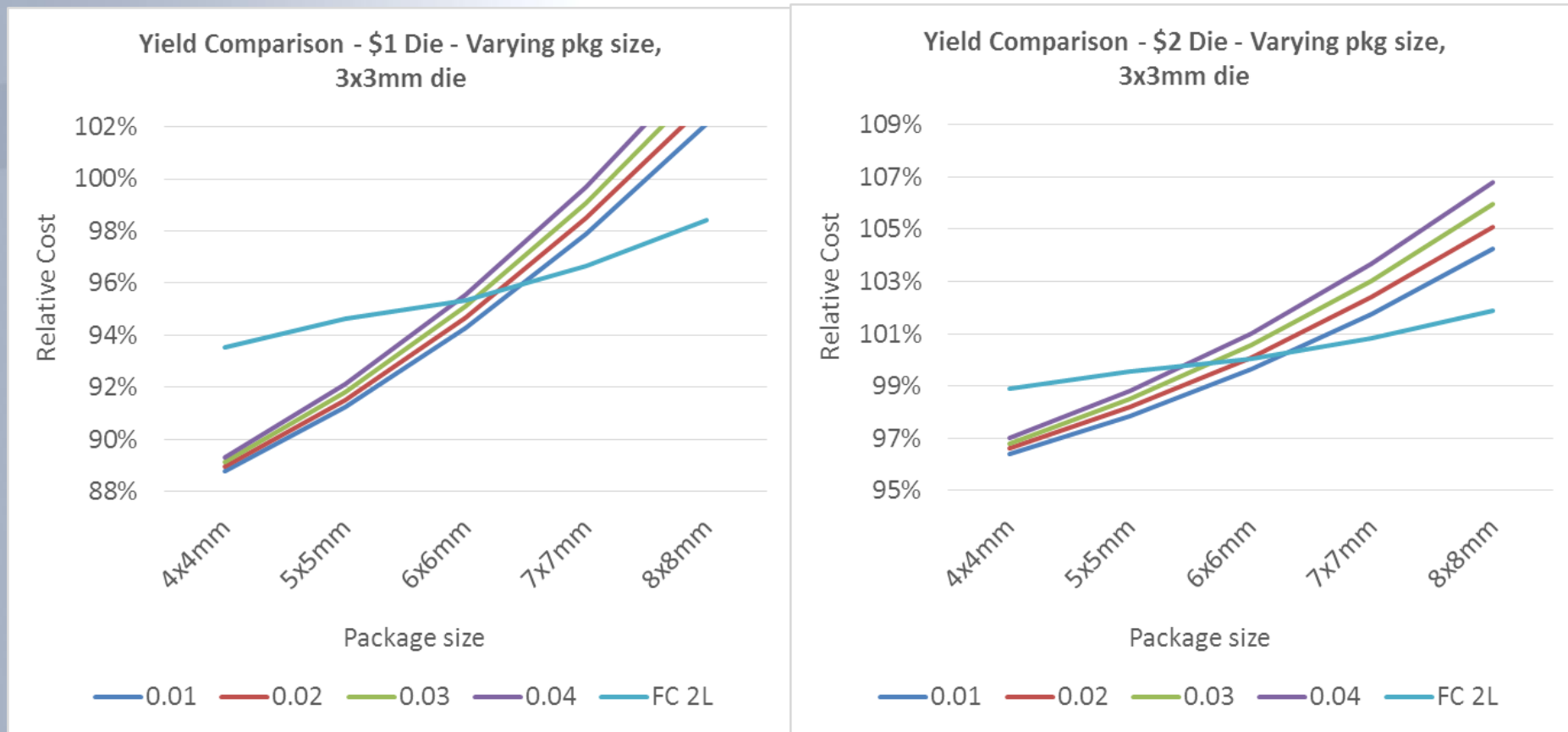
Yield Analysis – Varying Package Size

Conclusions based on processing costs only indicated FC packaging tends to be cost-effective for larger packages → Yield analysis further reinforces this

Yield Comparison - $1 Die - Varying pkg size, 3x3mm die

Yield Comparison - $2 Die - Varying pkg size, 3x3mm die

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Yield Analysis – Varying Package Size

Yield analysis also shows that the more expensive the die being packaged, the more likely FC packaging will be cost-effective
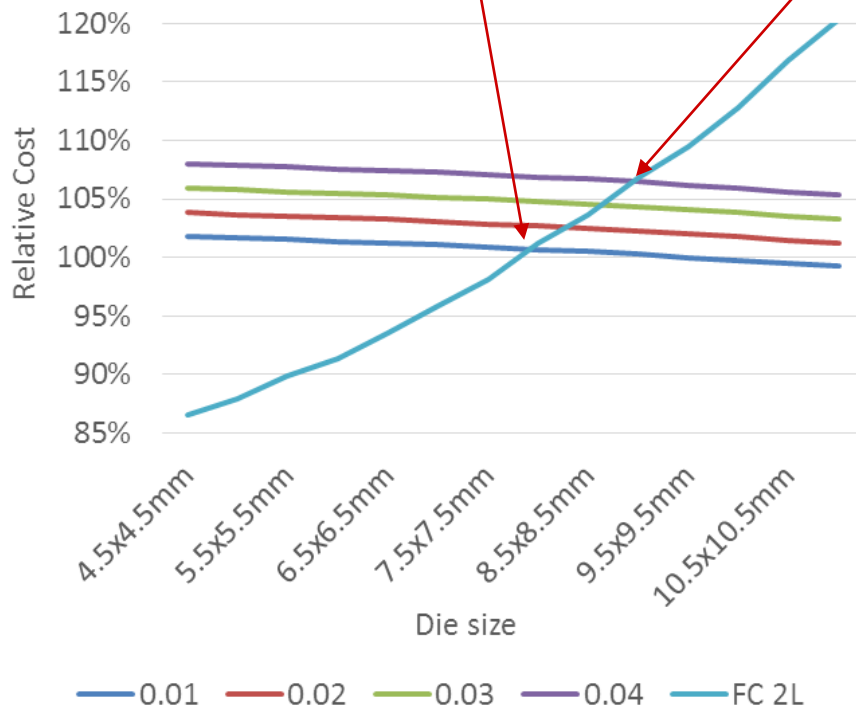
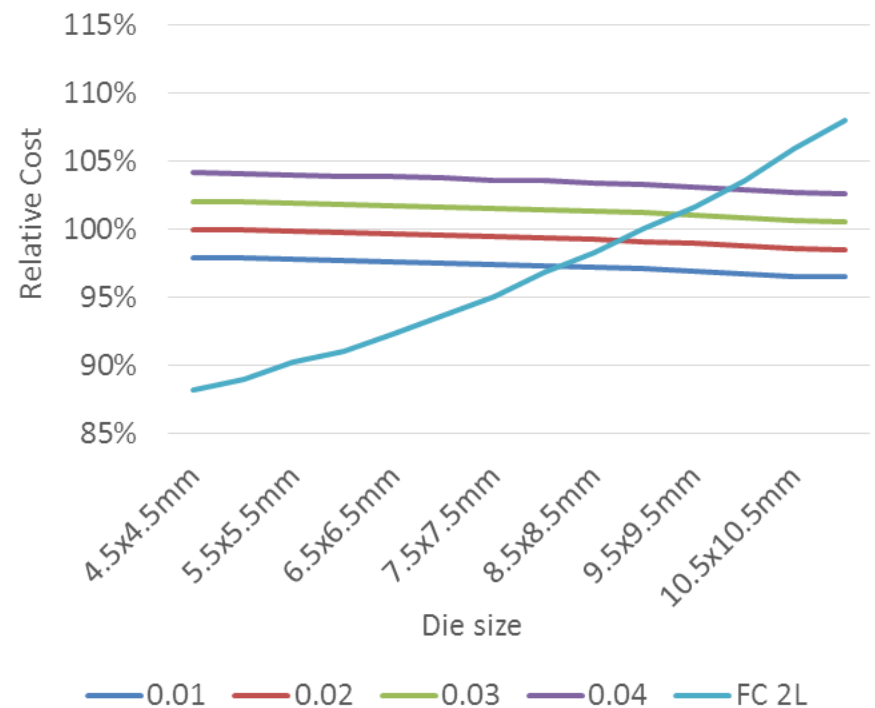IMAPS Device Packaging 2017

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Highest-yield FOWLP scenario is cost-effective starting at a 7.5x7.5mm die

Lowest-yield FOWLP scenario is cost-effective starting at a 8.5x8.5mm die

Yield Comparison - $1 die - Varying die, 13x13mm pkg

Yield Comparison - $2 die - Varying die, 13x13mm pkg
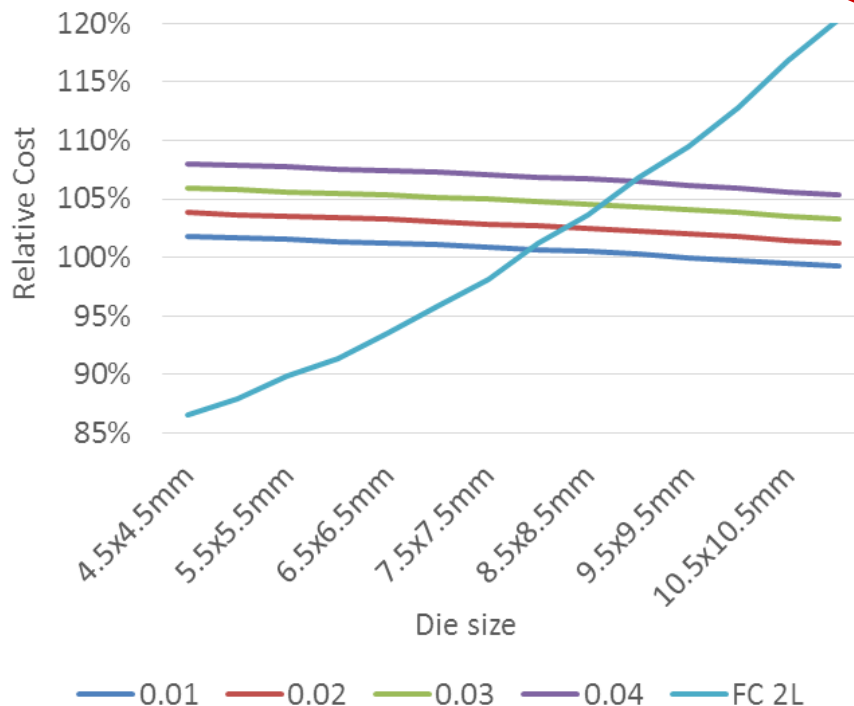
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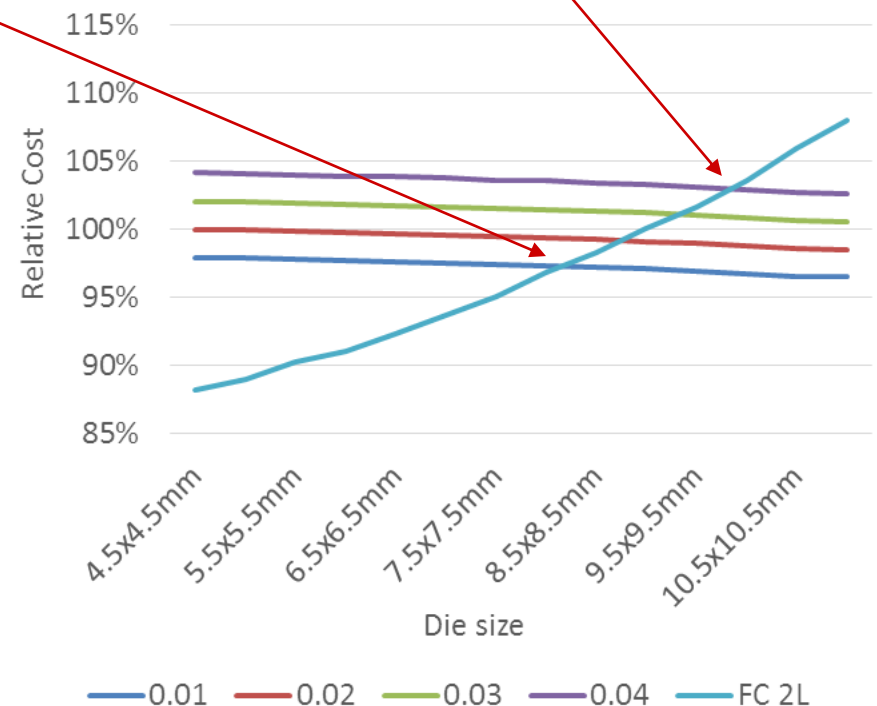
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Yield Analysis – Varying Die Size

Highest-yield FOWLP scenario is cost-effective starting at a 8x8mm die

Lowest-yield FOWLP scenario is cost-effective starting at a ~10x10mm die

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FOWLP not sensitive to die size, so all crossover point changes in these examples are based solely on yield changes → More expensive die has a range from 8x8mm to 10x10mm as to when FC is cost-effective

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Summary

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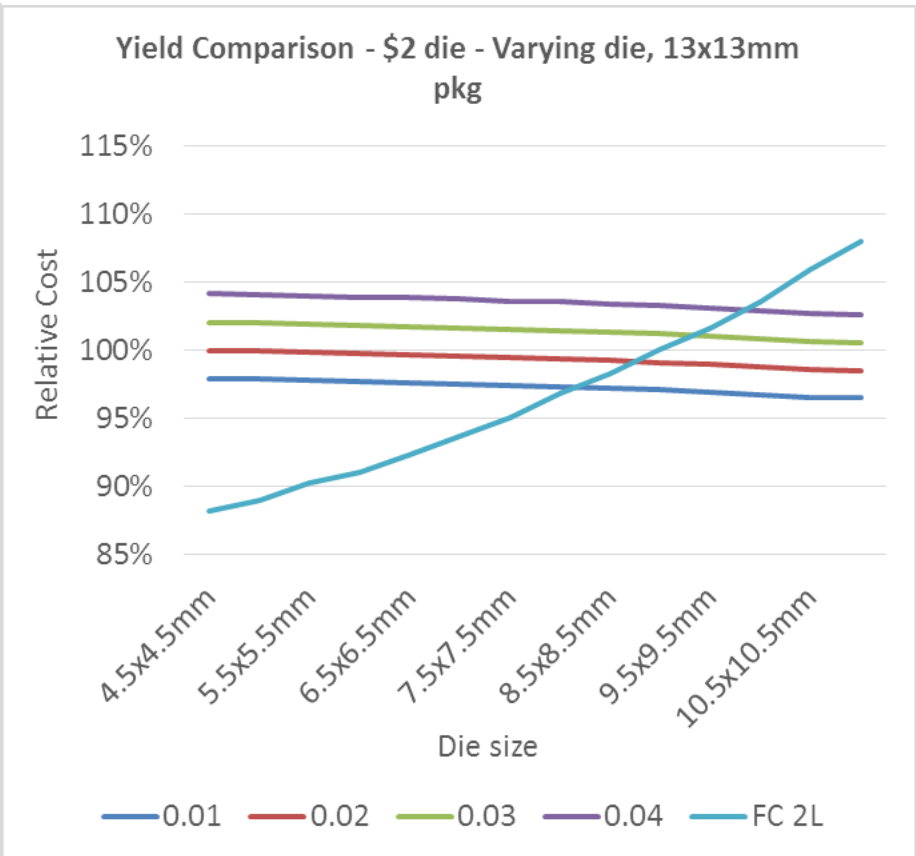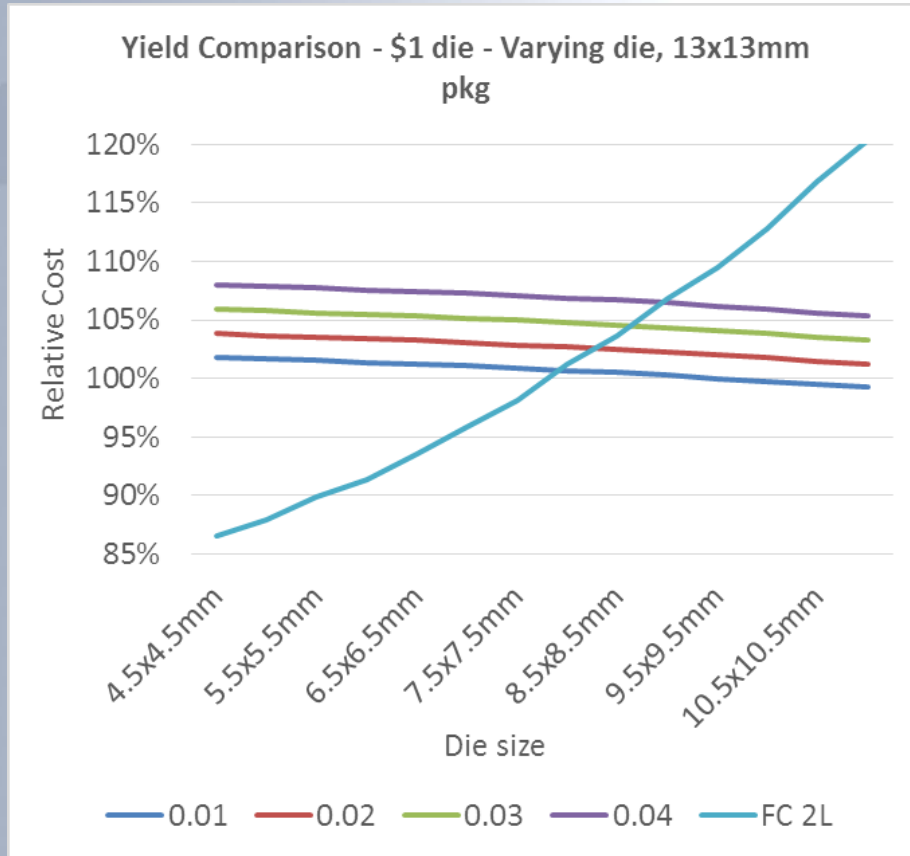
Summary

- **Yield is one key difference between FOWLP and flip chip packaging**
  - Three scrap points in the FC process, two scrap points for FOWLP

- **FOWLP is sensitive to package size**
  - Many activities are performed on the entire wafer at once → A larger package means fewer packages across which to amortize the batch cost

- **FOWLP is sensitive to die cost**
  - Due to having fewer scrap points
  - The more expensive the die, the more quickly FC becomes cost-effective

- **Flip chip is sensitive to die size**
  - Cost to bump a wafer is not insignificant → The larger the incoming die size, the higher the bumping cost associated with that die

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