Fabrication and Assembly Yield for Embedded Passives
Risks and Opportunities

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Abstract
This paper provides an overview of yield issues for embedded passives fabrication and assembly. The polymer thick film process for embedded resistors is used as an example of a typical embedded passives process, and opportunities for yield decrease and increase are discussed and compared to a corresponding discrete resistor board fabrication and assembly process. A general modeling methodology and technology (*SavanSys*) for predicting, measuring, and managing yield and cost is also described.

Economic Drivers for Embedded Passives
Accurately predicting the cost difference between a design with embedded passives and that same design implemented with discrete passives is difficult. There are many factors contributing to this difficulty, but one of the principal issues is that embedding changes the cost of both the board fabrication and board assembly. Another contributing factor to this challenge is the confidentiality of the real costs involved. In a typical product, design, board assembly, and board fabrication are done by three different companies, and each wants to maximize their profit. Pricing between these three companies will significantly affect the eventual cost that each of these companies pays.

In order to understand the difference between the cost of a board with embedded passives and the cost of the same board using discrete passives, it is helpful look at which costs are affected and the rate at which they change. For example, adding two discrete capacitors to a design will cost twice as much as adding one discrete capacitor. However, with some thin film (or laminate) type of embedded capacitor technologies, the cost of two embedded capacitors on a board is almost the same as the cost of one embedded capacitor. This is due to the fact that the cost of a capacitive layer pair is incurred on a per panel basis, not per device. There is also a test cost increase and a laser trim cost increase, the latter of which may be very large if additional probe cards are needed. In addition, there are screen printable discrete capacitor materials which will have additional material costs associated with them, and if the capacitors are printed with different pastes, there will be a major cost increase. Similar rules apply to embedded resistor technologies. The cost drivers for embedded passives can be grouped into the following three categories:

1. Increased board fabrication cost – The primary drivers that increase the board fabrication cost when embedding passives are increased material costs (especially for thin film materials) and the addition of extra processing steps. Much of the cost associated with the extra processing steps is incurred on a per panel basis. This is significantly different from the cost of adding a discrete passive, and if this difference is not considered, it will lead to sub-optimal designs. Adding two discrete passives to a design will cost approximately twice as much as adding one discrete passive. However, for thin film materials, the per panel fabrication cost of one embedded passive or two embedded passives--or even one thousand embedded passives--is approximately the same. Laser trimming and test costs will be proportional to the number of devices.

2. Decreased board assembly and component cost – Since the embedded devices replace discrete devices, the cost of assembling the board is reduced. The direct cost improvements include the cost of the replaced components plus the cost of placing those components on the board. Additionally, a board with embedded devices will have higher yield and reliability due to fewer solder joints. A significant reduction in the board assembly cost may be achieved for boards that can be converted from two sides to a single side.

3. Decreased board size/cost – In many cases, the surface real estate for placing components is the limiting factor on board size. In these designs, the use of embedded passives may result in a smaller board. If the size reduction is

enough to yield more boards per panel, the board fabrication cost of the embedded design may be less than the non-embedded option even though the cost per square inch of embedding is higher.

Fabrication and Assembly Yield

Yield and cost cannot be separated. The eventual cost of either a board fabrication process or an assembly process is the product of the final yield and cost. Using the definitions below for the different steps of the production process, it is possible to accurately model and track the cost and yield at each step in this process.

Following are the definitions for the board fabrication process. Since the majority of the board fabrication process is done on panels, the definitions below are given in terms of panels. However, these definitions may also be applied to individual boards.

- *Material step* – Any step in the manufacturing process that adds material to the panel. Defects in the added material are accumulated in the panel being processed.
- *Process step* – Any step in the manufacturing process that modifies some aspect of the panel. All processing steps have the opportunity to introduce additional defects to the panel.
- *Test step* – Any step which detects defects that have been added during previous material or processing steps. The test coverage defines the percentage of defects that are detectable in a given test step.
- *Rework step* – Any step which repairs defects in a panel. Success rate defines the percentage of defects which can be repaired.
- *Defects* – Problems that cause the panel to fail. For this paper, irregularities in material characteristics or processing which do not cause a circuit failure are not considered defects. For example, irregularities in the carbon paste which are compensated during trimming are not considered defects.
- *Defect Density* – The defect density will either be in terms of defects per square cm for area based defects or defects per million opportunities (DPMO) for activity based defects.
- *Yield* – Yield is the percent of defect free panels at any given in the process. The cumulative effect on yield of a particular processing step is given by the equations in Figure 1 below.

$$\text{AREA DEFECTS : } Yield_{Out} = Yield_{In} * (1 - \text{Defect Density})^{Area}$$

$$\text{ACTIVITY DEFECTS : } Yield_{Out} = Yield_{In} * (1 - DPMO / 1000000)^{\#\text{ of activities}}$$

Figure 1 – Yield and Defects

For the board assembly process, the definitions used in this paper are:

- *Component step* - Any step in the assembly process that adds components to the board. Defects in the added components are accumulated in the board being assembled.
- *Assembly step* – Any step in the manufacturing process that modifies some aspect of the board. All assembly steps have the opportunity to introduce defects to the system.
- *Test step* – Any step which detects defects that have been added during previous assembly steps or through faulty components. The test coverage defines the percentage of defects that are detectable in a given test step.
- *Rework step* – Any step which repairs boards with defects. Success rate defines the percentage of defects which can be repaired.
- *Defects* – Problems that cause the board to fail. For this paper, irregularities in the assembly process which do not cause the board to fail are not considered defects.
- *Defect Density* – The defect density is presented in terms of defects per million opportunities (DPMO) for the assembly process.
- *Yield* – Yield is the percent of defect free boards at any step in the process. The cumulative effect on yield of a particular assembly step is given by the activity defect equation in figure 1.

While some of the terminology between board fabrication and board assembly differs in the above definitions, the concepts are basically the same. From a yield management perspective, processing steps and assembly steps are equivalent, and material steps are the same as component steps. Additionally, the effect on yield of area based defect density and activity based defect density is the same. For example, the yield of a 100 sq.cm. board with a defect density of .001 per sq.cm. is the same as the yield of a board with 100 devices when each device has a defect density of 1000 DPMO. The yield for both of these cases is 90.48%.

Using the above definitions, a model of the complete process flow can be created to get the accurate yielded cost of any product being produced. First, the process flow is divided into a series of steps which are measured and quantified for yield and cost. Next, the results of each step are combined to produce the final yielded cost of the system.

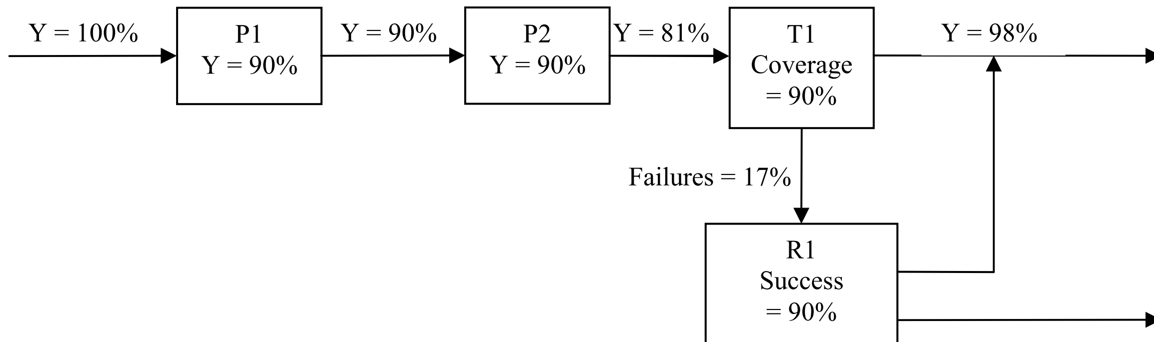

Figure 2 – Processing, Test, and Rework Process

The example in Figure 2 shows how the yield changes through a fabrication or an assembly process which includes test and rework steps. At the start of the process, the yield is 100% and the yield of process P1 is 90%. The yield of any step can be calculated using either area based defect density or activity based defect density as defined in the last section. The outgoing yield is the product of the incoming yield multiplied by the step yield. The same calculations are applied to P2, except the outgoing yield is now the product of the incoming yield (90%) and the step yield (90%) resulting in a new outgoing yield of 81%. A test step T1 with a coverage of 90% divides the boards (or panels) into ones that pass and ones that fail. The boards that pass continue through the production process, while the ones that fail are sent to rework R1. The yield of the passing boards now improves to 98%, since 90% of the defects are detected and eliminated from the batch of boards being produced. The rework step fixes 90% of these defects, and the repaired boards are put back into the main production flow having the same yield as those boards which passed the initial test step. 1.7% of the boards are scrapped in this flow, and the full cost of these scrapped boards must be allocated to the remaining good boards.

Since there are hundreds of processing steps and many test steps in a full board fabrication and assembly flow, the series of steps shown in the diagram is duplicated and combined several times to produce a complete yield model of the complete board production flow. This model tracks the yield as it goes up and down throughout the process. Understanding the yield at many key points in the process is crucial for yield improvement, as well as to optimize the test strategy.

The Impact of Embedded Passives on Fabrication and Assembly Yield for Polymer Thick Film (PTF) Embedding

As described in the previous section, any assembly or processing step can lower the yield of the design. In this section, specific issues related directly to the polymer thick film process (PTF) are analyzed for yield impact. One of the key aspects of PTF yield management is an examination of the relationship between the defects per resistor and defects per board or panel. Since defective resistors cannot be reworked once laminated, and so result in scrapping either the board or panel, the only way that embedded PTF resistors can be economical is for the defects per resistor to be extremely low. (Note that in this paper, we are treating the laser trimming step as a processing step required for all resistors. It is possible to consider laser trimming as a rework operation, but not for the purpose of this paper. Also, there are applications for PTF embedded passives which do not require laser trimming.) The board yield or panel yield is the percentage of each that has all the resistors within the required pre-trim tolerance limits.

A. Paste quality - The quality of the paste is extremely important. Printing conditions must be tightly specified. For example, viscosity must be within specification. More importantly, the sheet resistivity must be as close to the specified value as possible, and this is often a characteristic property of the process and depends on the final thickness of the embedded resistor component. Problems in the paste composition or mismatches in the sheet resistance are variables that must be eliminated to insure that the fabricated resistor value is within the tolerance range.

B. Resistor dimensions - The resistor dimensions have to be the larger in proportion to the copper thickness. Eighteen microns or thinner copper is preferred, but if the resistor dimensions are large enough, a thickness of thirty five microns is adequate. If thick copper is combined with small dimensions, termination effects will change the resistor values, and control over paste thickness and uniformity between terminations becomes more challenging.

C. Termination pad material - The termination pad material is also important. It has been shown[1] that pure copper termination offers poor reliability and stability. Better stability and less variation in the resistance value distribution are gained if the terminal pads are covered with silver or gold. Screen printed silver has proven to be the best material, but plated silver or gold can also be used, and they offer better registration than screen printed silver.

D. Registration Issues - Registration and compensation are other sources of potential yield problems. The resistor length is defined by photolithography (except if screen printed silver is used for terminations), and is affected by the typical board inner layer process tolerances. Under-etching of copper must be compensated, and variations in the etching process will cause variation in the resistor length. Since resistor length variations result in changes to the resistor value, this must be carefully controlled. In order to meet acceptable tolerances in the width, the mesh count of the stencil/screen must be as large as possible. For example, if a typical 325# (inch-based) mesh is used, there will only be four holes for the paste for a resistor that is 300 microns wide. Also, the material of the stencil/screen must be dimensionally stable to minimize the alignment problems. Alignment problems will cause serious yield decrease if there isn't enough overlap between the paste and the terminal pads.

E. Nonlinearity of resistor values - It is fairly easy to observe the nonlinearity of the resistance value of resistors with different dimensions. The length and width primarily fix the value, but not always as precisely as the resistivity equation predicts. In order to manage these nonlinear effects, a small number of different aspect ratios should be used. This is a typical process related issue, in which the yield should increase as more experience with the process is gained. The potential sources for this kind of yield decrease are the screen printing and the curing of the paste. Uncontrolled curing may cause great variations in the resistance value distributions.

F. Trimming - Trimming resistors is a relatively easy way to keep yields high. Laser trimming adds cost to the process, but in most cases this extra cost is well worth it given the yield increases achieved. Laser trimming ablates the resistive material and increases the total resistance value. Tight tolerances are easily achieved, but trimming has to be taken into account when the circuit is being designed. Since trimming increases the value, the resistor values must be designed lower than target value.

G. Fewer board solder joints – Unlike A through F above, which all reduce the yield of an embedded design as compared to the equivalent discrete version, the assembly process of a board with embedded passives is actually better than one with discrete resistors. A major driver of assembly yield is the total number of solder joints per board. Embedded passives have no solder joints compared to discrete passives, which have two. Therefore, embedding one hundred resistors eliminates two hundred solder joints.

Test and Scrap Strategy – Panel vs. Boards

The decision to scrap an entire panel, or continue processing that panel and scrap individual bad boards after the panel has been routed into boards, is crucial for optimizing the total cost. The optimal panel vs. board scrapping decision depends on the following four factors:

- $\mathbf{Cost_{Test}}$ - The total labor, material, tooling, and equipment cost invested in the panel through the test step.
- $\mathbf{Cost_{Routing}}$ - The total remaining labor, material, tooling, and equipment cost from the test step through routing the panel into boards.
- $\mathbf{Y_{Panel}}$ - The panel yield. This is the percentage of panels that are defect free at this point in the processing.
- $\mathbf{Y_{Board}}$ – The board yield. This is the percentage of board that are defect free at this point in the processing.

If the cost invested in the board through the test step ($\mathbf{Cost_{Test}}$) is high in comparison with the remaining cost through routing the board ($\mathbf{Cost_{Routing}}$), marking and scrapping boards later should be considered. Another considerable factor is the yield difference between the board and the panel. If the board yield is high and the panel yield is low, marking and scrapping boards later in the process should be considered. The yield difference between the board and the panel is directly proportional to the number of boards per panel.

$$\text{COST OF SCRAPPING A PANEL}: (Y_{Panel} * Cost_{Test}) + Cost_{Routing}$$

$$\text{COST OF SCRAPPING A BOARD}: (Cost_{Routing} + Cost_{Test}) * Y_{Board}$$

$$\text{PANEL AND BOARD YIELD RELATIONSHIP}: Y_{Panel} = Y_{Board}^{\#\text{ of boards per panel}}$$

Figure 3 – Panel and Board Scrapping Cost

The equations shown in Figure 3 above illustrate the cost of both strategies. Each scenario can easily be constructed and analyzed using the step, yield, and defect definitions presented previously in this paper. By varying the location of the test and scrap step, the scenario that generates the lowest total cost should be adopted. For designs with a few boards per panel, the yield of the board and panel will be close. This scenario will tend to favor panel scrapping. However, if the number of boards per panel is quite high (which is common in many of today's embedded designs) board scrapping will be better.

While these equations are easy to describe and optimize, and the total cost invested and remaining is relatively easy to measure, the exact panel and board yield ($\mathbf{Y_{Board}}$ and $\mathbf{Y_{Panel}}$) is often difficult to determine. These yield figures are not the observed yield at the test step if test coverage is less than 100%. For this optimization to be done correctly, the real yield of the board and panel must be determined, and defects that are in the panel but not visible until some later test step must be counted as part of the panel and board yield at the time these defects are put into the system.

***SavanSys* Overview**

Below is a brief description of the *SavanSys* activity based cost and yield modeling technology. For additional information on the capabilities and availability of this technology, please contact the authors.

SavanSys is a cost, yield, and technology tradeoff tool. Data is extracted from the design tool environment to create a physical representation of the design. Activity based models of both board fabrication and assembly are created to model the manufacturing process using the step definitions presented earlier in this paper. This combination of design and manufacturing information is used to generate a "virtual prototype" of the board to accurately determine size, cost, and yield throughout the manufacturing process. The results of this model are extremely accurate because it considers the details of the target board applied to a specific manufacturing environment with precise costs and yields.

The data considered by *SavanSys* for doing this analysis is listed below.

The Design Model in SavanSys

Because of the substantial number of packaging technologies, processes, and materials that are available, making optimum choices is not a trivial task. Alternative technologies and materials include:

- Substrates (printed circuit boards, ceramic, thin-film, etc.)
- Chip packaging
- Bonding techniques (wirebond, TAB, flip chip)
- Test techniques
- Manufacturing methods

SavanSys accepts physical information that describes multiple chips (or bare die) and their interconnection. All of the information that is collected by *SavanSys* is physical, as opposed to logical, behavioral, or functional. *SavanSys* does not import VHDL or similar behavioral information because such descriptions do not contain a significant amount of useful physical information. *SavanSys* inputs and considers the following physical inputs.

Chips (bare die and packaged die):

- Dimensions (length, width, thickness)
- I/O type and count
- Cost and yield

Chip Packaging:

- Bonding (technology, materials, and design rules)
- Encapsulation (materials and design rules)
- Die attach (materials and design rules)
- Process flow information (chip preparation, testing, and burn-in)

Boards/Modules:

- Substrate (technology, materials, and design rules)
- Connectorization (technology, materials, and design rules)
- Process flow information (substrate fabrication)

In *SavanSys*, netlists are optional because tradeoff activities often take place prior to the presence of a detailed netlist. Therefore, the total number of nets in a partition can be estimated with *SavanSys* even without a detailed netlist.

Module size prediction is accomplished by computing the following set of footprints for each component (active and passive) in the board.

- The interconnect-capacity footprint is the size limitation based on the amount of wiring required to connect a component within the module. It depends on the wiring capacity of the substrate and the quality of the routing.
- The via-density footprint accounts for the number of vias that are available to connect component I/O to wiring layers.
- The bond-pad-density footprint accounts for the distribution of bond pads on the surface of the interconnecting substrate.
- The escape-routing footprint analyzes routing component I/O out from under the die, either to wiring tracks on the surface of substrates or to vias that connect to other wiring layers.
- The placement or die footprint represents the physical size of the bare die or packaged chip and its surrounding bonds, as well as minimum spacing to adjacent components.

In order to obtain the module area, the footprints representing each component are appropriately accumulated. The plot in Figure 4 shows the results of a *SavanSys* analysis.

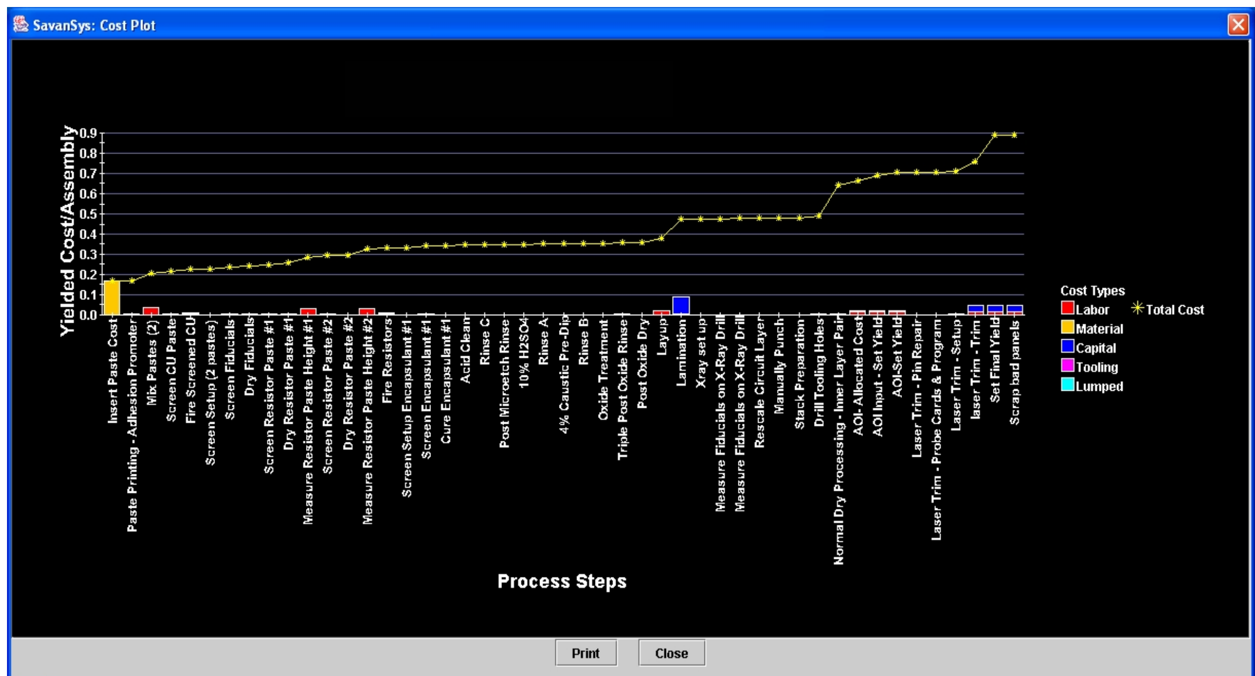

Figure 4 - Cost Plot

The Manufacturing Model in SavanSys

SavanSys cost models may include the following costs and yield. Given that the costs below are optional, *SavanSys* models can be used to analyze total system costs or specific components of the system cost.

- Component cost and yield (entered or computed)
- Component preparation (process may be defined)
- Single chip package cost and yield (entered or computed)
- Substrate fabrication cost and yield (entered, computed, or process flow)
- Surface mount and through-hole assembly cost and yield
- Bare die attach cost and yield (TAB, wirebond, flip chip)
- Tooling costs associated with assembly processes
- Test, repair, and rework costs, coverages, success rates, and yields.

The methodology for defining cost models in *SavanSys* is based on dividing the process into a series of activities and then defining the costs, times, and yields associated with each of those activities. Step types in *SavanSys* are one of the following:

- Substrate – This step calculates the cost and yield of the substrate using either a user defined calculation or running a substrate fabrication process flow.
- Component – This type of step adds the cost and yield of new components to a system.
- Assembly – This type of step is used to define the cost and yield of board assembly activities.
- Processing – This type of step is used to define the cost and yield of board fabrication activities.
- Test - This type of step defines testing activities. Defects introduced into the system by previous steps are detected by test steps, and the board/panel is either fixed through rework or scrapped.
- Rework – This type of step defines the repair or rework activities.

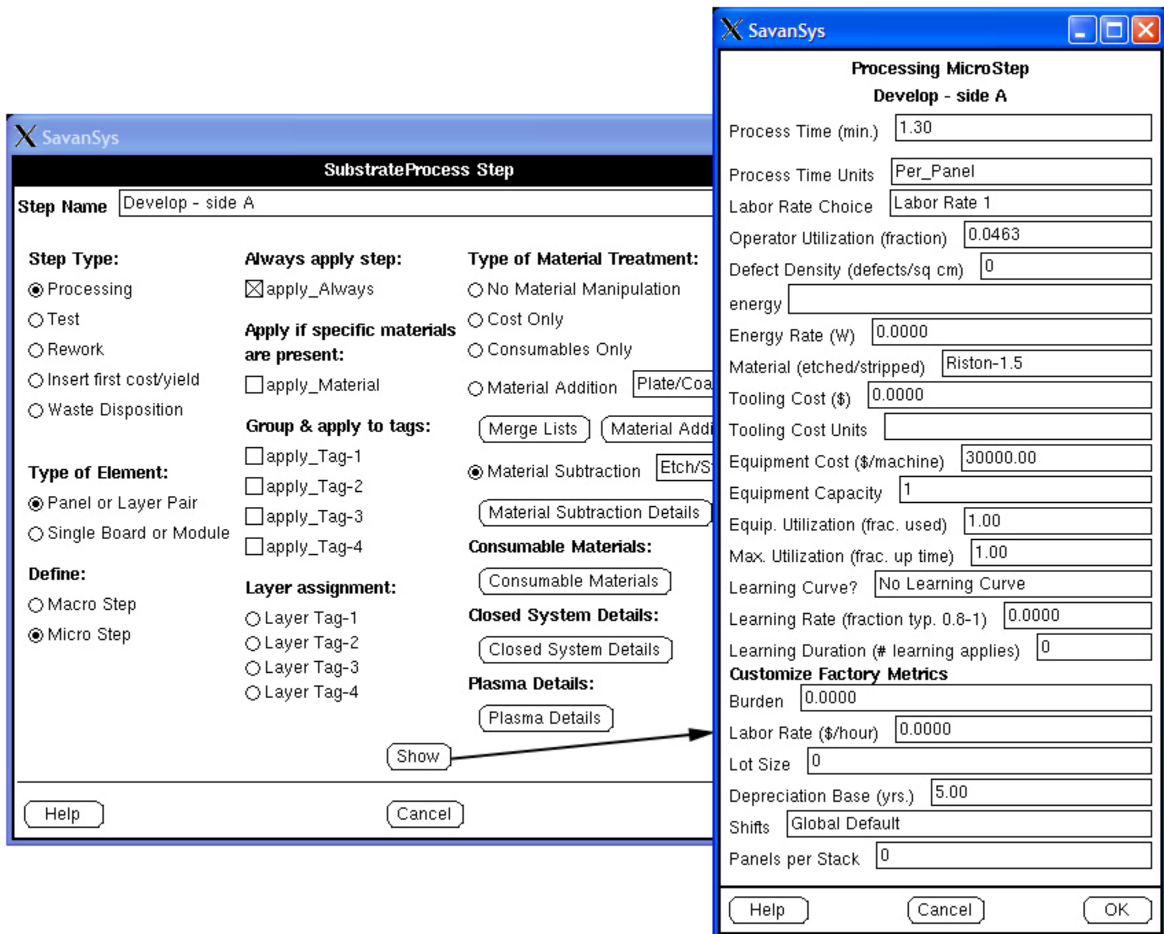

Figure 5 – Develop Step Details

Step definitions in *SavanSys* vary slightly based on the type of step, but all steps include the following basic information:

- Time – Used to calculate labor and equipment costs.
- Operator utilization and rate – Combined with time to get cost.
- Equipment utilization and cost – Combined with time and depreciation schedule to determine allocated cost.
- Defects in parts per million or defects per square cm – Used to calculate and accumulate the system yield.
- Tooling costs – Divided over the lifetime quantity of boards.
- Material and amount used – References the material database to calculate material costs.

The screen shot in Figure 5 shows an example step definition for a develop step.

Yield Improvement Suggestions

Given the issues presented, below are suggestions for keeping the yield as high as possible for designs using embedded PTF resistors. One general concept which is part of many of the suggestions below is that a key factor for high yield PTF production is repeated achievement of a tight range of resistance values. To a large degree, it doesn't matter what the mean of this resistance range is as long as it is repeatable and tight. Trimming is used to achieve the final resistance value, and once this mean and range is determined, the circuit design can be adjusted accordingly to ensure that all resistors are trimmed up to their target value. Activities which increase the range of resistance should be avoided, while activities which reduce the range of resistance should be adopted.

A. Carefully manage the paste quality. Variations in viscosity, sheet resistivity, and contamination will result in a wide distribution of resistor values prior to trimming. While many of these variations can be fixed during trimming, it only takes one bad resistor to scrap the whole board or panel.

B. Keep the resistors as large as possible. In one sense this is opposite to the conventional yield optimization approach for board fabricators. Since board fabricators typically measure defect density in defects per sq. cm., the conventional wisdom is that smaller devices should give better yield. In fact, the exact opposite is true. Unlike silicon in an integrated circuit, carbon paste is not a crystalline structure, and one small imperfection in the paste is not necessarily a fatal defect. However, if the resistor is quite small, this imperfection in the paste begins to appear rather large and may be fatal. In addition, larger resistors help the yield by making registration easier. Of course, there is a limit to this approach, and when one is embedding many resistors, the area for each resistor will be limited. However, if space is available, yields will be improved if the resistors are made larger as opposed to automatically using minimum size devices.

C. Avoid too small or too large aspect ratios. Differences in the termination effects will broaden the pre-trim range of resistor values.

D. Use as few different aspect ratio resistors as possible. While nonlinearities in the observed resistance will still occur, by using the same aspect ratios, these nonlinearities will track together. As discussed in the beginning of this section, if resistance values track together, the resistance range will be tighter and more easily compensated during design.

E. Measure the resistance and range of the fabricated resistors and adjust your design and processing practices accordingly. This seems a bit obvious, but there is a large benefit to doing this for PTF embedded designs. As discussed, the pre-trimmed resistor value does not have to be precise, it simply should be repeatable and consistent. If your processing activities stay the same, you will tend to get the same results. As discussed previously, there are a number of factors concerning the quality, viscosity, and application of the paste which will affect the pre-trimmed resistor value. Once the board fabricator adopts and repeats the same activities, the results will be the same, and this fact should be used to optimize the production yield of embedded PTF designs.

6. Choose the optimal panel versus board scrapping strategy. Embedding is an inner layer process. Historically, most inner layer processes have been a small percentage of the total board cost, and panel scrapping when finding a defect has been the normal procedure. However, significant cost and yield hits are now part of the PTF inner layer process, and panel scrapping is not always the best approach.

7. Use thin copper. Since paste is put on a surface with copper, the thicker the copper, the more irregular the surface. Therefore, the paste application will be more irregular if it is applied to an irregular surface, particularly when small dimensions are required. These irregularities will cause significant resistance variations and risk

pushing some of the values outside the trimmable range. However, if the resistor dimensions are large enough, the copper thickness (18μm vs. 35 μm) is not crucial.

Summary and Conclusions

Yield must be measured and managed for embedded passives production to be economical. Unfortunately, yield is much harder to measure than production cost because defects are only observed later in the process, and the exact cause of the defect is not always clear. However, by adopting the approaches above and by performing repeated experiments and root cause analysis, board fabricators can achieve good yields for many embedded designs.

The only accurate method for comparing the true cost of an embedded passives design to a discrete passives design is to consider both the additional yield challenges for embedding, as well as the yield improvement of the assembly process.

[1]Gregory Dunn, John Savic, Troy Bachman, Remy Chelini and Tim Dean, "Improvements in Polymer Thick Film (PTF) Resistor Technology." CircuiTree July 2003.